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Third Interim Report

812269

EXPANDED LITTLE IDA PROGRAM INSTRUMENTATION

Ross M. Chapman
Raymond J. Coates
Edward K. Mofford, et al
General Electric Company

TECHNICAL REPORT NO. RADC-TR-66-719
February 1967

Rome Air Development Center
Research and Technology Division
Air Force Systems Command
Griffiss Air Force Base, New York

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FOREWORD

This technical documentary report is the result of the efforts of a number of contributors, who each had a significant part in writing various portions of this document. The editorial responsibility for this report was assigned to Raymond J. Coates. These contributors were:

Ross M. Chapman	Nicolas E. Vicoli
Raymond J. Coates	Robert D. Wengenroth
Edward K. Mofford	Eugene D. Wurdinger
Matthew R. Scalzetti	Joseph H. Yamaoka

Report was prepared under Contract No. AF30(602)-3946 by General Electric Company, Advance Projects Development Operation, Heavy Military Electronics Department, Syracuse, New York. The contract was initiated under Project 5582, Task 558202. Mr. Robert A. Mather (EMASA) was the RADC project engineer.

This document is not releasable to CFSTI because it contains information embargoed from release to Sino-Soviet Bloc Countries by AFR 400-10, "Strategic Trade Control Program."

This technical report has been reviewed and is approved.

Approved: Robert A. Mather
ROBERT A. MATHER
Project Engineer

Approved: Joseph Fallik
JOSEPH FALLIK
Chief, Space Surveillance and
Instrumentation Branch
Surveillance & Control Division

ABSTRACT

The interim report describes the work performed in providing new instrumentation under U.S. Air Force Contract AF30(602)-3946, from 15 March 1966 to 15 September 1966. The Expanded Little IDA Program is a continuation, as well as an expansion, of the effort previously carried out under U.S. Air Force Contract AF30(602)-3360 to investigate the characteristics of ionospherically propagated HF signals. The long-term objective of these studies is to provide more accurate estimates of the major environmental factors needed for over-the-horizon system design. The equipment described in this report is being designed and installed to provide the proper tools to meet these objectives.

The overall block diagrams for the three transmitter sites and the common receiver site are discussed in Section I. Equipment developments are discussed separately in subsequent sections. Each of these sections contains a general description of what is to be built, the results to date in meeting the design goals, and the design details of each equipment being built by General Electric. For those equipments whose design construction are complete, installation, alignment, and operating instructions are included. The equipment discussed in this report includes HF antennas, high dynamic range HF receiver, digital processor, mode processor, absolute time equipment, HF ionospheric sounders, Phantom pulse compression system, and test and communication equipment.

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SECTION I

INTRODUCTION

This technical documentary report reviews work (performed from 15 March to 15 September 1966 on U.S. Air Force Contract AF30(602)-3946 under supervision of the Rome Air Development Center) which will provide instrumentation for the Expanded Little IDA Program. The long term objective of this program is to provide more accurate estimates of the major environmental factors needed for over-the-horizon radar (OHR) system design. The experiment design, data reduction, and data analysis being performed under this contract have been discussed in Interim Report No. 2 on this program.[1] This program is a continuation, as well as expansion, of the effort previously carried out under U.S. Air Force Contract AF30(602)-3360, also directed by the Rome Air Development Center, to determine the characteristics of ionospherically propagated high frequency (HF) signals. Consequently, some of the required instrumentation is already in place and operating.

The new instrumentation to be provided on this program falls into three categories: (1) the equipment required at the central receiver site for more automated data collection, improved performance, and new experiments, (2) the equipment required at the present Coco Solo, Canal Zone transmitter site for improved performance, and (3) the equipment required to instrument the two new transmitter sites. When the instrumentation is complete, the two new transmitter installations and the existing transmitter site will be functionally identical; therefore, all three transmitter sites will be discussed together.

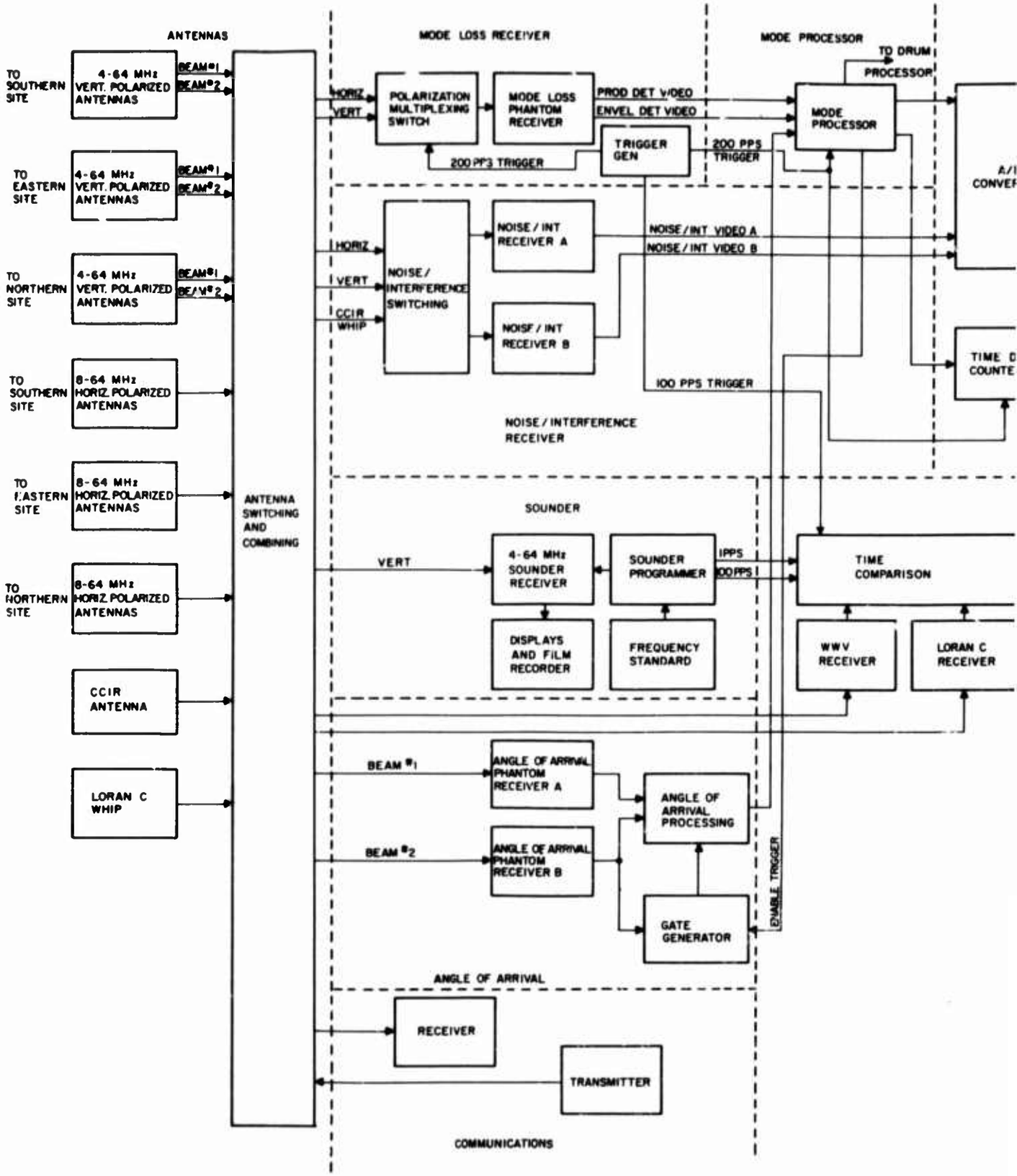
1. RECEIVER SITE

A functional block diagram of the receiver site is shown in Figure 1. This block diagram was discussed in detail in Interim Report No. 1.[2] Since it is basically unchanged, that discussion will not be repeated here.

Starr Hill -- near Remsen, New York -- has been selected as the new receiver site. This selection followed an intensive review of other sites within a reasonable distance of Rome, New York. While this site is being developed, operations are continuing at the existing site near Stockbridge, New York. The reasons for the move from Stockbridge to Starr Hill include the capability to employ the downward slope of Starr Hill to obtain antennas with low angle gain at a reasonable cost. The new instrumentation that is available before Starr Hill is complete is being installed and checked out at Stockbridge. This equipment, together with the existing units, will then be moved to Starr Hill when the facilities and antennas are ready.

2. TRANSMITTER SITES

The functional block diagram of a transmitter site is shown in Figure 2. This block diagram was also discussed in Interim Report No. 1, but is included here for reference. One of the original objectives of the Expanded Little IDA Program was to instrument three transmitter sites, oriented north, south, and east of the central receiver site. As mentioned before, the existing station at Coco Solo, Canal Zone is being updated and will continue to be used as the southern site. Pingorssuit ("P") Mountain at Thule, Greenland has been selected for the northern site. No location has yet been selected as an eastern site. Negotiations are still in progress with the foreign government involved for permission to make a site selection survey.


ANTENNAS
TO SOUTHERN SITE
4-64 MHz VERT. POLARIZED ANTENNAS
BEAM #1
BEAM #2
TO EASTERN SITE
4-64 MHz VERT. POLARIZED ANTENNAS
BEAM #1
BEAM #2
TO NORTHERN SITE
4-64 MHz VERT. POLARIZED ANTENNAS
BEAM #1
BEAM #2
TO SOUTHERN SITE
8-64 MHz HORIZ. POLARIZED ANTENNAS
TO EASTERN SITE
8-64 MHz HORIZ. POLARIZED ANTENNAS
TO NORTHERN SITE
8-64 MHz HORIZ. POLARIZED ANTENNAS
CCIR ANTENNA
LORAN C WHIP
ANTENNA SWITCHING AND COMBINING
MODE LOSS RECEIVER
HORIZ
VERT
POLARIZATION MULTIPLEXING SWITCH
MODE LOSS PHANTOM RECEIVER
PROD DET VIDEO
ENVEL DET VIDEO
200 PPS TRIGGER
TRIGGER GEN
200 PPS TRIGGER
MODE PROCESSOR
TO DRUM PROCESSOR
MODE PROCESSOR
A/D CONVER
HORIZ
VERT
CCIR WHIP
NOISE / INTERFERENCE SWITCHING
NOISE / INT RECEIVER A
NOISE / INT RECEIVER B
NOISE / INT VIDEO A
NOISE / INT VIDEO B
TIME D COUNTE
100 PPS TRIGGER
NOISE / INTERFERENCE RECEIVER
SOUNDER
VERT
4-64 MHz SOUNDER RECEIVER
SOUNDER PROGRAMMER
1PPS
100PPS
TIME COMPARISON
DISPLAYS AND FILM RECORDER
FREQUENCY STANDARD
WWV RECEIVER
LORAN C RECEIVER
BEAM #1
BEAM #2
ANGLE OF ARRIVAL PHANTOM RECEIVER A
ANGLE OF ARRIVAL PHANTOM RECEIVER B
ANGLE OF ARRIVAL PROCESSING
GATE GENERATOR
ENABLE TRIGGER
ANGLE OF ARRIVAL
RECEIVER
TRANSMITTER
COMMUNICATIONS

1

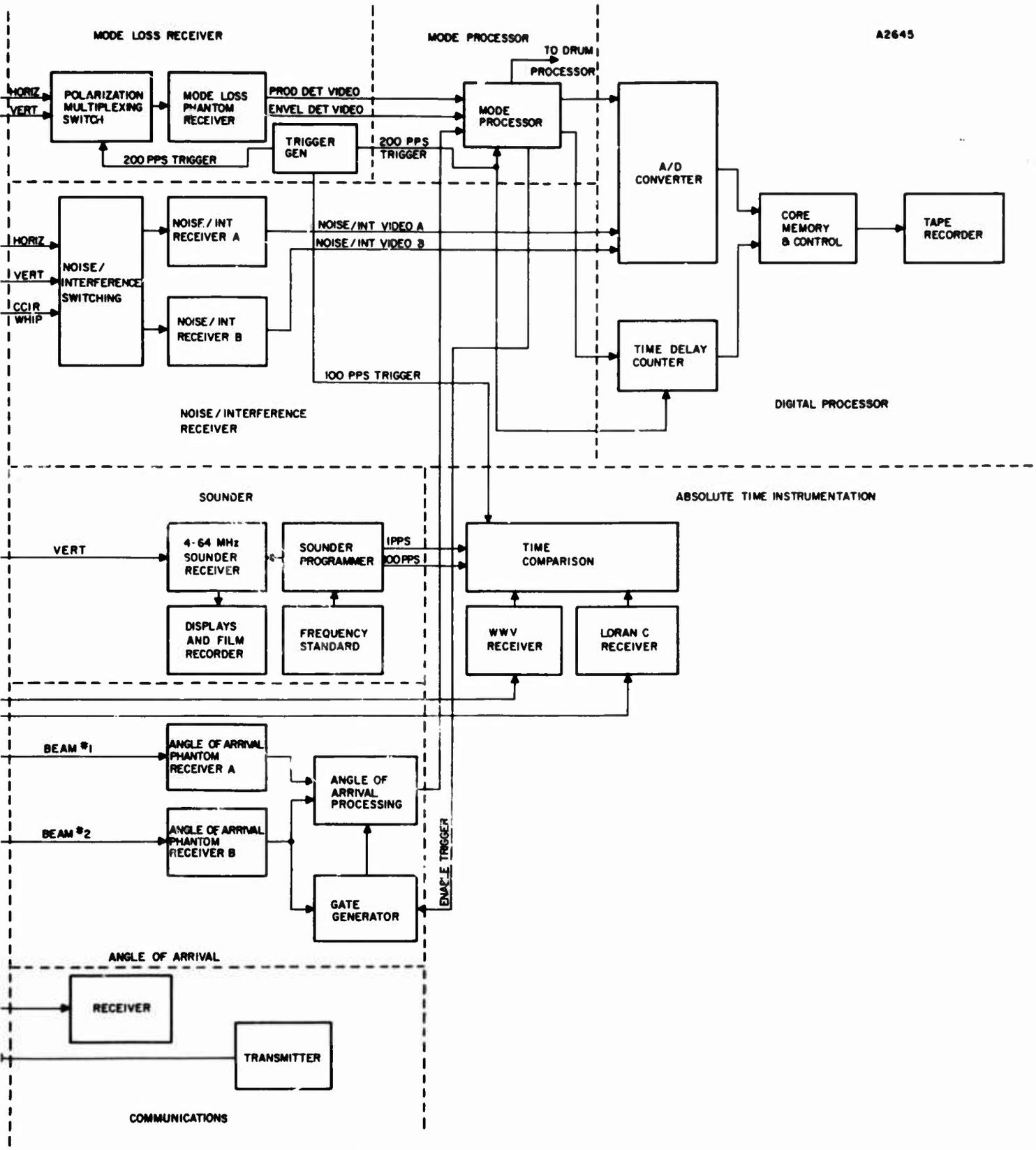
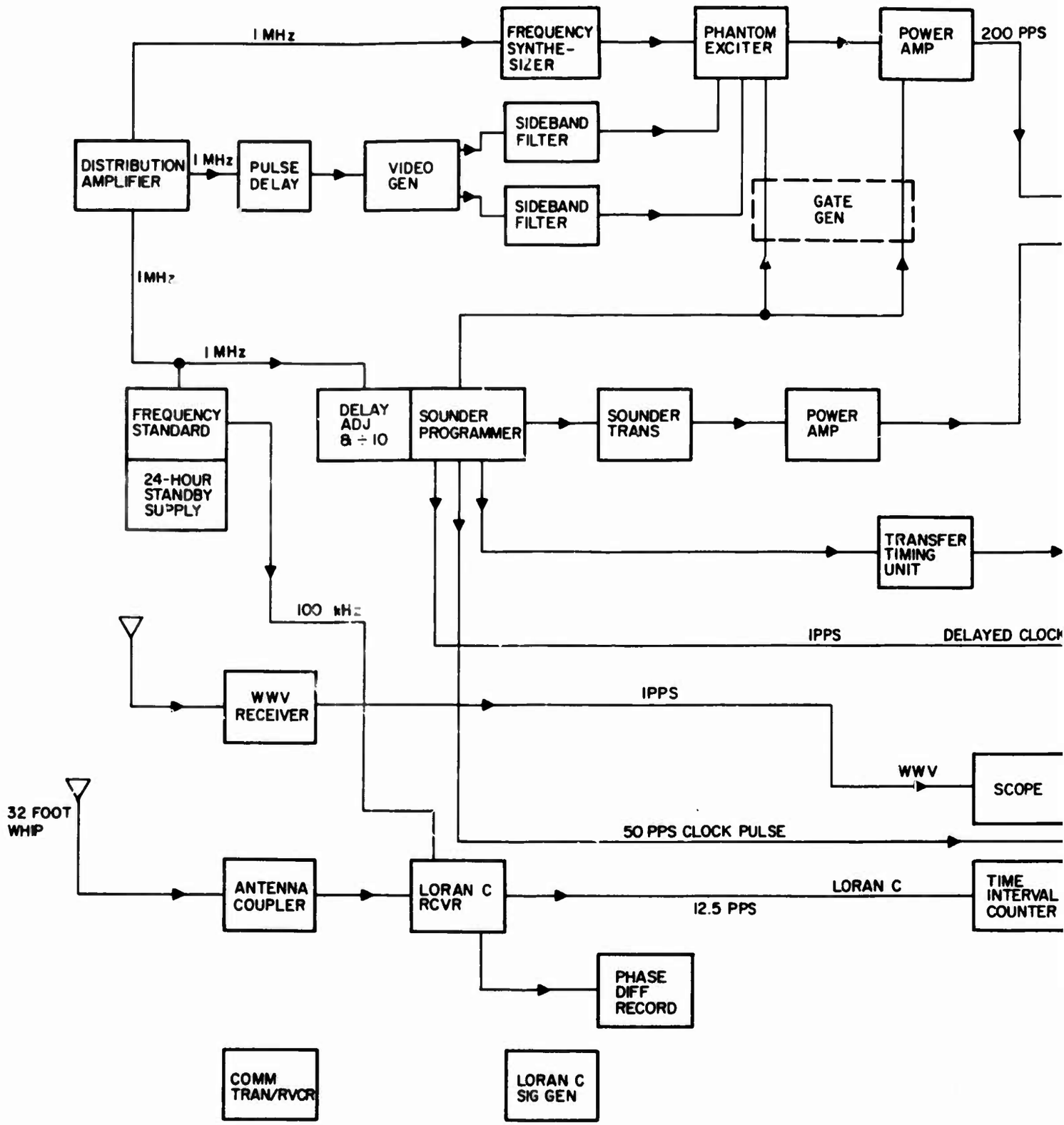


Figure 1. Receiver Site


1 MHz
FREQUENCY SYNTHE-SIZER
PHANTOM EXCITER
POWER AMP
200 PPS
SIDEBAND FILTER
DISTRIBUTION AMPLIFIER
1 MHz
PULSE DELAY
VIDEO GEN
SIDEBAND FILTER
GATE GEN
1 MHz
1 MHz
FREQUENCY STANDARD
24-HOUR STANDBY SUPPLY
DELAY ADJ & ÷ 10
SOUNDER PROGRAMMER
SOUNDER TRANS
POWER AMP
TRANSFER TIMING UNIT
100 kHz
1PPS
DELAYED CLOCK
WWV RECEIVER
1PPS
WWV
SCOPE
32 FOOT WHIP
50 PPS CLOCK PULSE
ANTENNA COUPLER
LORAN C RCVR
LORAN C
TIME INTERVAL COUNTER
12.5 PPS
PHASE DIFF RECORD
COMM TRAN/RVCR
LORAN C SIG GEN

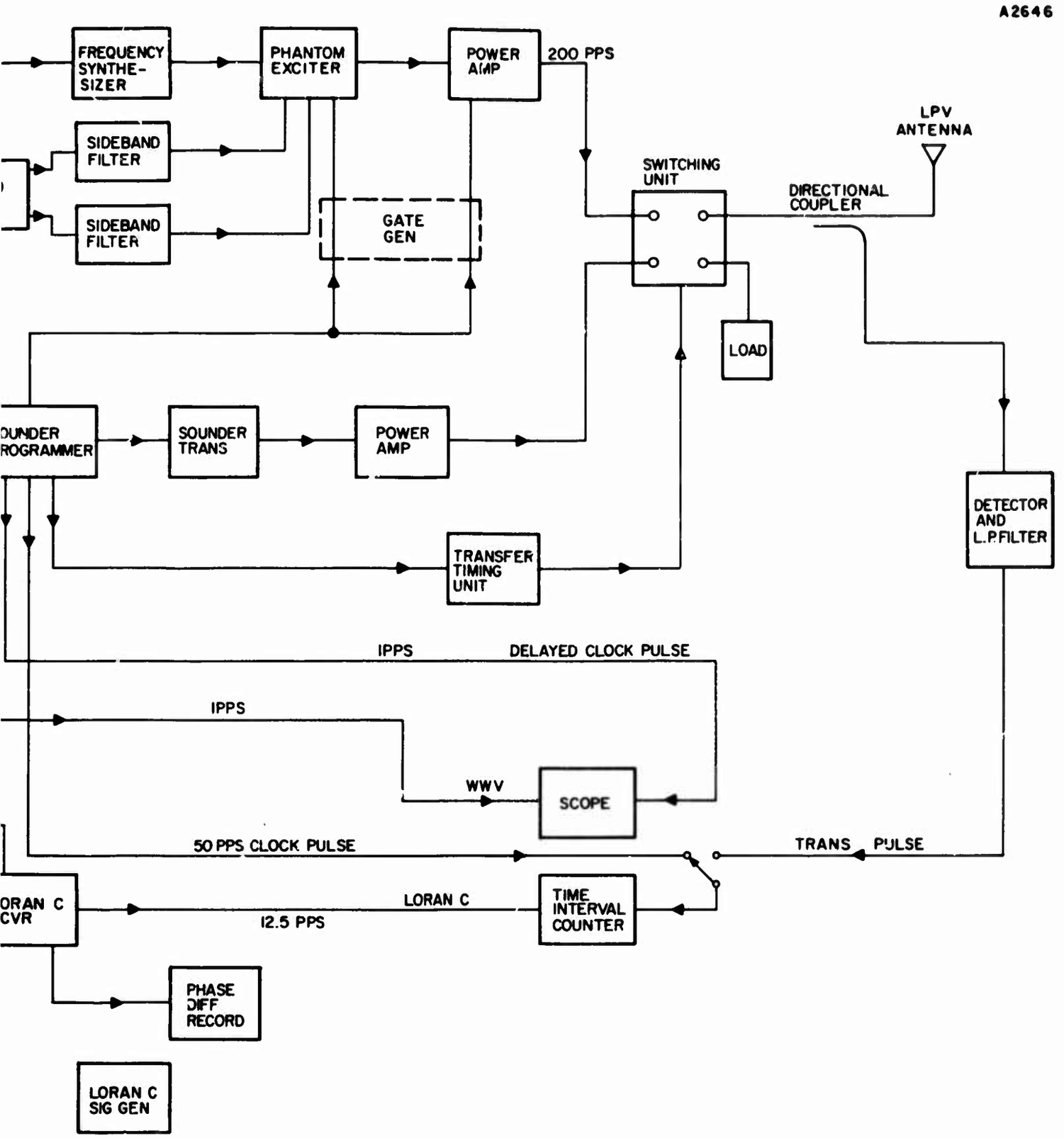


Figure 2. Transmitter Site

2

SECTION II

ANTENNAS

The status of work on the Expanded Little IDA antennas is given in this section. Because the installation and measurement of these antennas is incomplete, the full description and the calibration data are not yet available. These data will be presented in the final report.

1. STARR HILL RECEIVER SITE

Three antennas of the type described in Interim Report No. 1 have been ordered from the American Electronics Laboratory, Colmar, Pennsylvania. Similarly, the ground screen mesh was ordered from Erico Products, Inc., Cleveland, Ohio.

These receiver antennas are comprised of three curtains. Two vertical logarithmically-periodic dipole arrays are spaced about two-thirds wavelength apart at their phase centers and have their apexes at a common point. A dual horizontal logarithmically-periodic dipole has one curtain one-half wavelength above ground and the second curtain one wavelength above ground. The vertically polarized antennas are fed independently for angle-of-arrival measurements. The horizontal curtains are fed by a single line to form the desired elevation pattern. Three sets of these antennas will be installed, one facing each transmitter site. The specifications to which these antennas are being built is shown in Appendix A.

When originally proposed, the ground screen was to be laid directly on the ground as is the normal procedure for antennas of this type; however, it was realized that at Starr Hill, in the so-called snow belt area of central New York, a considerable depth of snow would accumulate during the winter. A study of the effects of this snow was undertaken. This study showed that snow on top of the ground screen could destroy its effect. A summary of this study is described in Appendix B. In order to avoid this problem, the ground screen must be installed at least four to six feet above ground level. An eight-foot height makes it possible to work below the screen in addition to avoiding the snow. While the installation of such a ground screen is obviously more expensive, this cost is partially balanced out by the fact that no grading of the terrain is now required. In planning for the construction and installation of such a screen, the decision was reached to make a set of mats, each 18 feet wide and 500 feet long; 96 of these mats are required. The spacing between individual ground wires will be two feet in both directions. Erico Products, Inc., has been contracted to perform this fabrication. The specification for this work is shown in Appendix C. These mats must then be erected 8 feet in the air and the 18-foot widths fastened together by compression fittings. The work specification for this construction is shown in Appendix D.

2. COCO SOLO TRANSMITTER SITE

The 4- to 32-MHz antenna curtain at the site in Coco Solo, Canal Zone, was replaced by a new, longer, logarithmically-periodic dipole array with a frequency range of 4 to 64 MHz. The new array is designed with the bottom of the elements about one foot above ground. Thus, the elevation pattern will be essentially frequency-independent. The antenna installation was completed in August, and the patterns measured by a team of RADC and General Electric personnel. The data from the tests had not been reduced at the time this report was written; preliminary inspection of the data indicates reasonable performance of the antenna in its environment.

3. THULE TRANSMITTER SITE

A Granger model 726 antenna from Camp Tuto at Thule was found to be available. RADC arranged for the Corps of Engineers to move these antennas to "P" Mountain, and to install the antennas and their transmission lines there. This installation is being completed at the end of this reporting period.

4. EASTERN SITE

There has been no action on antennas for an eastern site since the definitization of the exact site location is pending.

SECTION III

NOISE/INTERFERENCE RECEIVER

1. GENERAL DISCUSSION

The noise/interference receiver is comprised of both the analog and digital circuits necessary to collect noise and interfering signal amplitude data in the 4- to 40-MHz range. This dual-channel, double-conversion, superheterodyne receiver features electronic tuning, high dynamic range, and low spurious frequency content (in-band "birdies"). The design also includes complete self-checking and calibration capability. Basic design considerations have been discussed in Interim Report No. 1. The measured and/or predicted receiver performance as of this point in the development is presented in Table I. Also presented for comparison purposes are the original design objectives. Nearly all of the original design objectives have been met or exceeded. In particular, front-end, second-order intermodulation distortion has exceeded the specification by 25 dB. Second IF linearity has been improved from ±1.5 dB to ±0.5 dB over the 40-dB amplitude range of each IF amplifier.

It should be noted that intermodulation (IM) and cross-modulation (CM) terms are given relative to 10 mv input signals instead of the original 50 mv. This action has been taken to make the stated performance more meaningful relative to our present assessment of the environment.* The performance relative to other input levels may be found by changing the IM and CM levels by an amount equal to (N - 1) times the change in input signal voltage level in dB where N is the order number of the distortion. For example, changing the input signal level from 50 mv to 10 mv is a 14-dB change in input level. This results in a $(3-1) \times 14$ dB = 28 dB decrease in the third-order IM and CM product level.

As can be seen, the measured noise figure is about 6.5 dB high. This increase is attributable to (1) higher RF filter loss (6 dB instead of the originally assumed 4 dB per four-pole filter section at 40 MHz), (2) higher RF amplifier noise figure (8.5 dB rather than the assumed 6 dB), and (3) significant input directional coupler, switching, and cabling loss. While the noise figure is somewhat high, it is recommended that the experiment proceed with the equipment as it now performs. Should the data indicate a lower noise figure requirement at the high frequency end of the band, there are several alternatives that may be considered for improvement. Some of these are (1) broadening the response

* "HF Receiver Investigation," study being conducted by General Electric for RADC on Contract AF30(602)-4194.

TABLE I

RECEIVER ELECTRICAL PERFORMANCE

Item	Nominal Design Objectives	Measured or Presently Predicted Performance
Front-end dynamic range		
All products from two 10-mv rms signals (CW or 100% AM) shall produce		
Second-order intermodulation	-89 dB	-114 dB
Third-order intermodulation	-103 dB	-98 dB
Third-order cross-modulation	-103 dB	-104 dB
Linear operating range	120 dB	120 dB
Noise Figure	10 dB nominal	16.5 dB nominal
Image rejection	-80 dB	-80 dB
IF rejection	-80 dB	-80 dB
Input impedance	50 Ω	50 Ω
Second IF linearity (over a 40-dB amplitude range)	±1.5 dB	±0.5 dB
Post-detection integration period	0.3, 3.0, and 500 sec.	0.3, 3.0, and 500 sec.
Overall receiver bandwidth (-6 dB)	4.0 kHz	4.0 kHz
Tuning	All electronic (remote or manual)	All electronic (remote or manual)
Calibration capability	By self-contained equipment	By self-contained equipment

of the front-end filters (at high end of band only) to reduce insertion loss, (2) modifying the front-end filters (different transfer function, reduction in number of poles, higher Q coils, etc.), and (3) redesigning the RF amplifier for a lower noise figure.

The first of these alternatives might be accomplished by interchanging filter boards in the field. This change will compromise the image rejection performance of the receiver, but early data collection experience may indicate that this compromise is warranted.

Several changes have been incorporated in the receiver design since Interim Report No. 1 as a result of evolving system performance specifications and design problems encountered during the breadboard test phase. These changes have been incorporated into the receiver block diagram shown in Figure 3 and are described below.

A single first mixer was incorporated in the design (rather than the three shown previously) when it was determined that the intermodulation distortion performance of the mixer circuit designed to perform the first mixing step could not be improved significantly by limiting the frequency range of the RF signal input to the mixer.

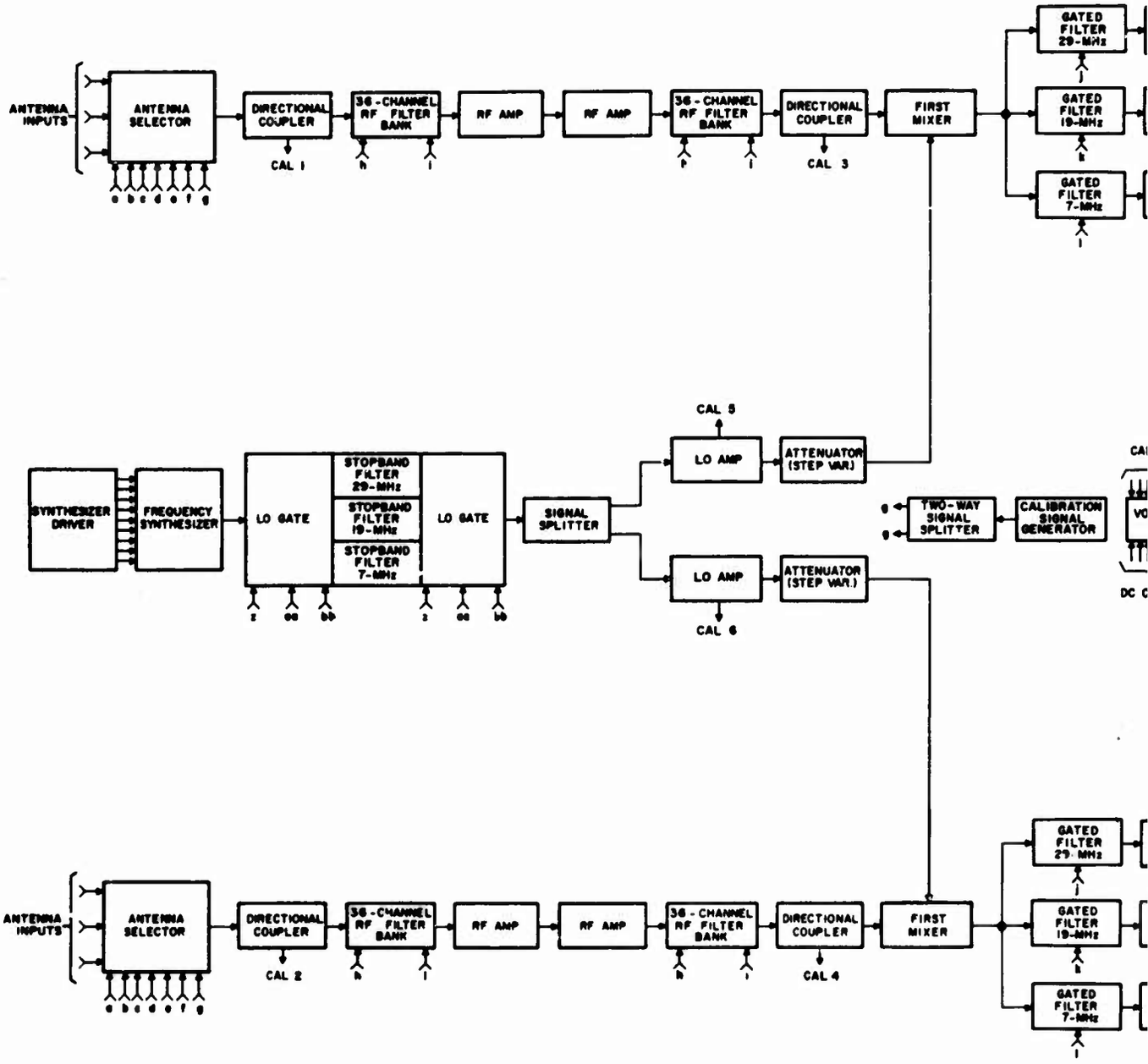
Three filters were added after the first mixing step (one each at 29, 19, and 7 MHz) to prevent the high-level local oscillator (LO) signal from desensitizing the first IF amplifier stage.

Two additions were made to provide capability not previously incorporated in the receiver. First, a 500-second integration period was added to the 0.3-second and 3-second integration periods already provided. Second, an additional remotely selectable crystal filter was added to the second IF portion of each receiver channel to provide a 1-kHz receiver bandwidth in addition to the 4-kHz bandwidth already available. Both of these additions were made to facilitate comparison of the data gathered on the Expanded Little IDA Program using the noise/interference receiver with data gathered by the International Radio Consultative Committee (CCIR).

An audio output has been provided to the operator to allow for aural monitoring of both receiver channels.

The second LO portion of the receiver was modified to provide frequencies derived independently of the HP 5100A frequency synthesizer which furnishes the first LO signal. This change was made to reduce equipment complexity.

The digital portion of the noise/interference receiver has encountered no difficulties of a technical nature in development to date.


ANTENNA INPUTS
ANTENNA SELECTOR
a b c d e f g
DIRECTIONAL COUPLER
CAL 1
36 - CHANNEL RF FILTER BANK
h
i
RF AMP
RF AMP
36 - CHANNEL RF FILTER BANK
h
i
DIRECTIONAL COUPLER
CAL 3
FIRST MIXER
GATED FILTER 29-MHz
j
GATED FILTER 19-MHz
k
GATED FILTER 7-MHz
l
SYNTHESIZER DRIVER
FREQUENCY SYNTHESIZER
LO GATE
STOPBAND FILTER 29-MHz
STOPBAND FILTER 19-MHz
STOPBAND FILTER 7-MHz
LO GATE
z
aa
bb
SIGNAL SPLITTER
CAL 5
LO AMP
ATTENUATOR (STEP VAR.)
LO AMP
ATTENUATOR (STEP VAR.)
CAL 6
TWO-WAY SIGNAL SPLITTER
CALIBRATION SIGNAL GENERATOR
ANTENNA INPUTS
ANTENNA SELECTOR
a b c d e f g
DIRECTIONAL COUPLER
CAL 2
36 - CHANNEL RF FILTER BANK
h
i
RF AMP
RF AMP
36 - CHANNEL RF FILTER BANK
h
i
DIRECTIONAL COUPLER
CAL 4
FIRST MIXER
GATED FILTER 29-MHz
j
GATED FILTER 19-MHz
k
GATED FILTER 7-MHz
l

1

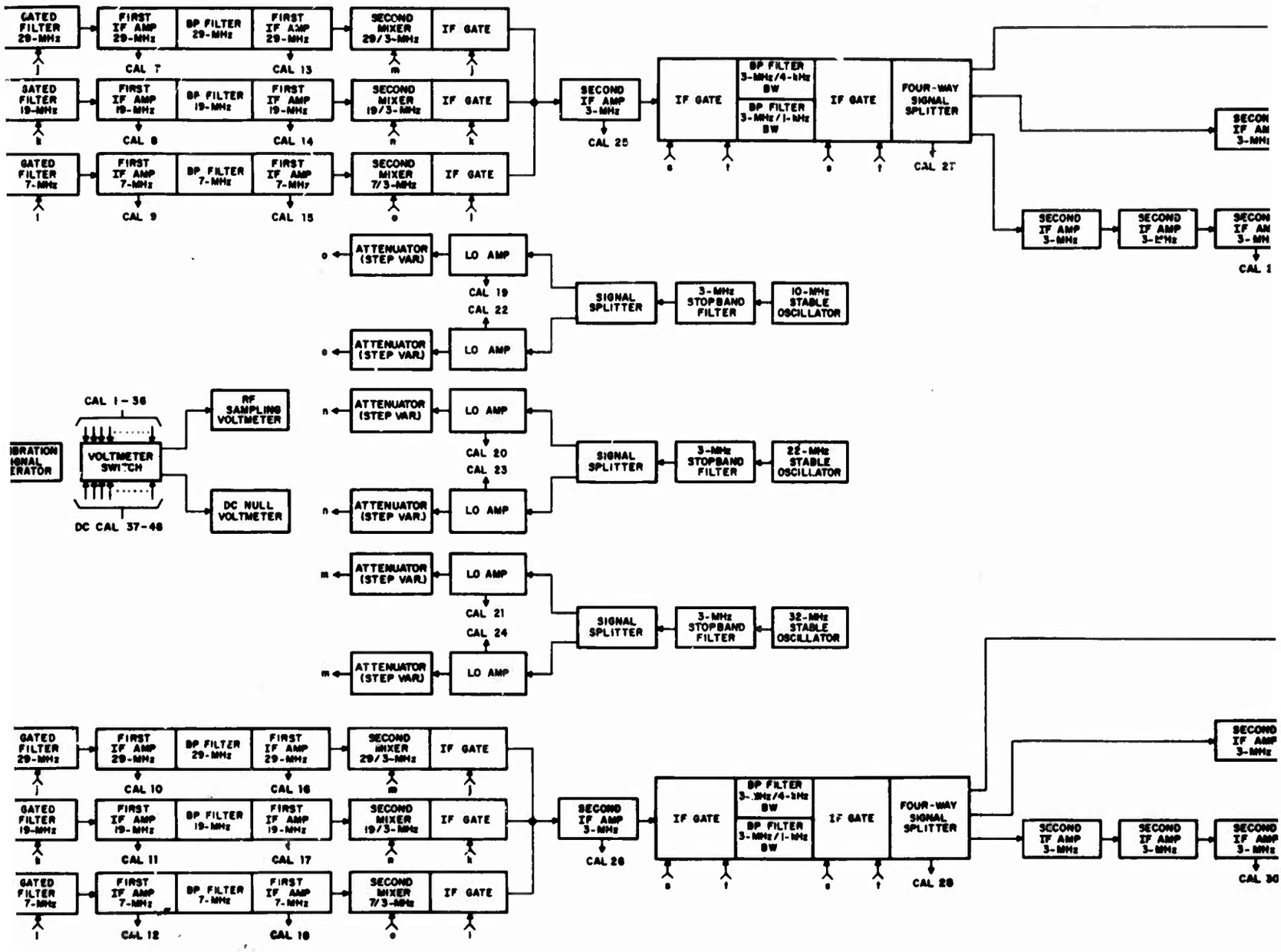
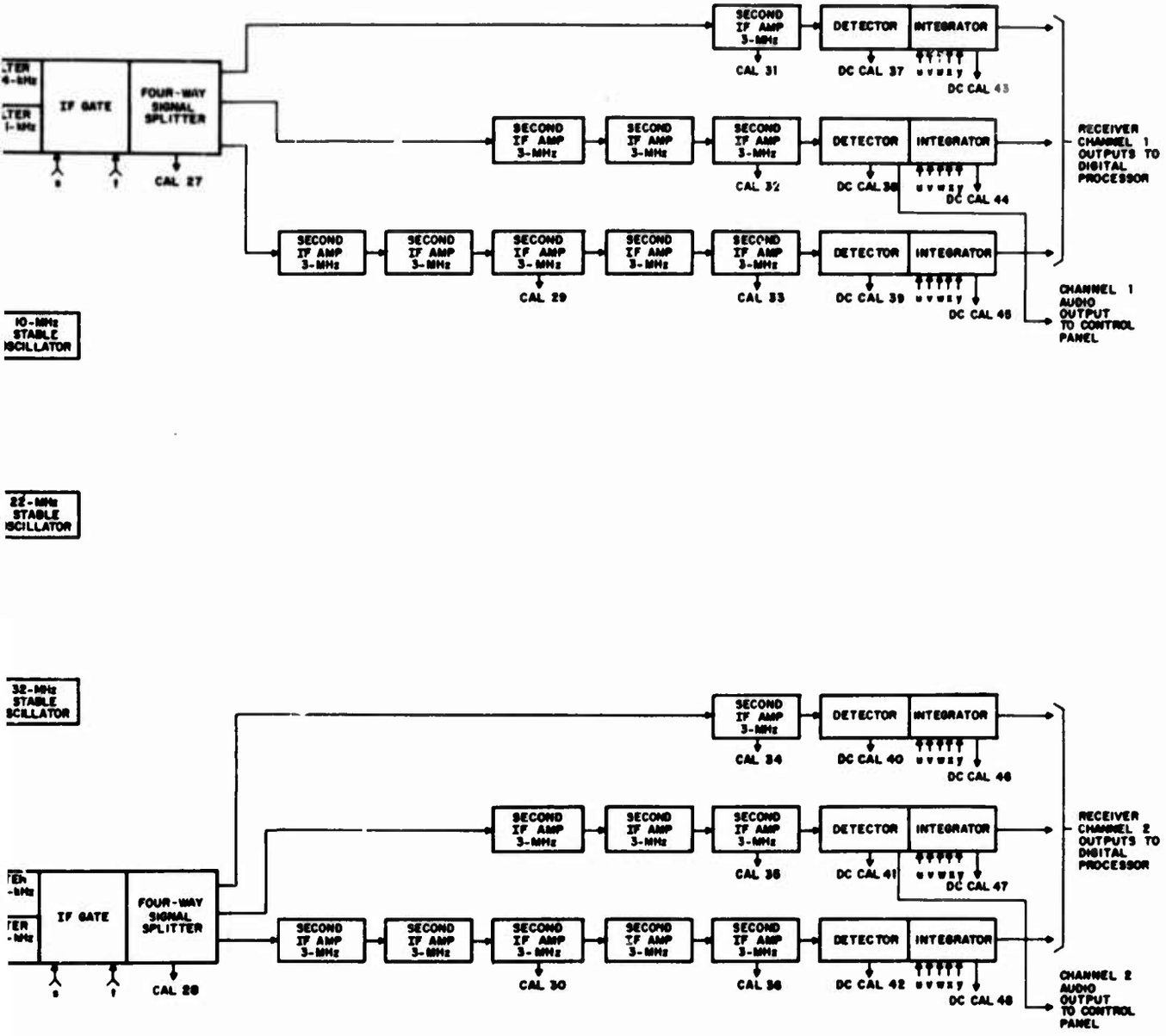


Figure 3. Analog Portion of Noise/ Interference Receiver


IF GATE
FOUR-WAY SIGNAL SPLITTER
CAL 27
SECOND IF AMP 3-MHz
DETECTOR
INTEGRATOR
CAL 31
DC CAL 37
DC CAL 43
CAL 32
DC CAL 38
DC CAL 44
CAL 29
CAL 33
DC CAL 39
DC CAL 45
RECEIVER CHANNEL 1 OUTPUTS TO DIGITAL PROCESSOR
CHANNEL 1 AUDIO OUTPUT TO CONTROL PANEL
STABLE OSCILLATOR
CAL 28
CAL 34
DC CAL 40
DC CAL 46
CAL 35
DC CAL 41
DC CAL 47
CAL 30
CAL 36
DC CAL 42
DC CAL 48
RECEIVER CHANNEL 2 OUTPUTS TO DIGITAL PROCESSOR
CHANNEL 2 AUDIO OUTPUT TO CONTROL PANEL

2. DETAILED DESCRIPTION OF ANALOG RECEIVER ELECTRICAL DESIGN

a. Receiver Front-End Unit

The receiver front-end unit incorporates the RF selectivity, RF amplification, first mixing, and post-mixer filtering functions, and is shown in block diagram form in Figure 4. This portion of the receiver accepts signals in the 4- to 40-MHz range and filters the signals in two banks of fixed-frequency bandpass filters. One bank of filters performs a preselection function while the other acts as an interstage filter bank between the RF amplifier stages and the mixer stage. After amplification in two RF amplifier stages which have been specially designed for a very high degree of linearity, desired signals are mixed to one of three IF's which has been selected for lowest in-band mixer spurious signal level. These three IF signal paths constitute the outputs of the receiver front-end unit.

(1) RF Filter Bank Design

The basic function of this portion of the equipment is to provide a means by which the receiver may be programmed electronically to examine a given increment of the 4- to 40-MHz RF range. The increment width was selected as 1 MHz at the 0.5-dB points; therefore, the development of this equipment requires that 36 individual filters be designed and incorporated so that the receiver frequency response could be switched to any given point in the overall range within an elapsed time of 2 ms. Switching isolation was required to be 80 dB minimum. Additional constraints were placed on the design of the filters by stipulating that the VSWR at the input to a bank of filters be less than 1.4 and the maximum loss of an individual filter be no greater than 4.5 dB. The filter shape factor was specified to be 8 maximum, where shape factor is defined to be the ratio of 60 dB BW/0.5 dB BW. In-band ripple of ±0.3 dB maximum was considered to be permissible.

The actual filter structure which was employed in the design, as well as the necessary design equations, are covered quite thoroughly in Interim Report No. 1, and therefore will not be reiterated here. The circuit configuration used is that shown in Figure 5. The overall block diagram of the RF filter bank is shown in Figure 6.

A major problem that was encountered in the development of the filter bank was the design of the switching matrix. As initially proposed, the individual filters incorporated an input and an output switch. This was discarded in the initial design phases since this

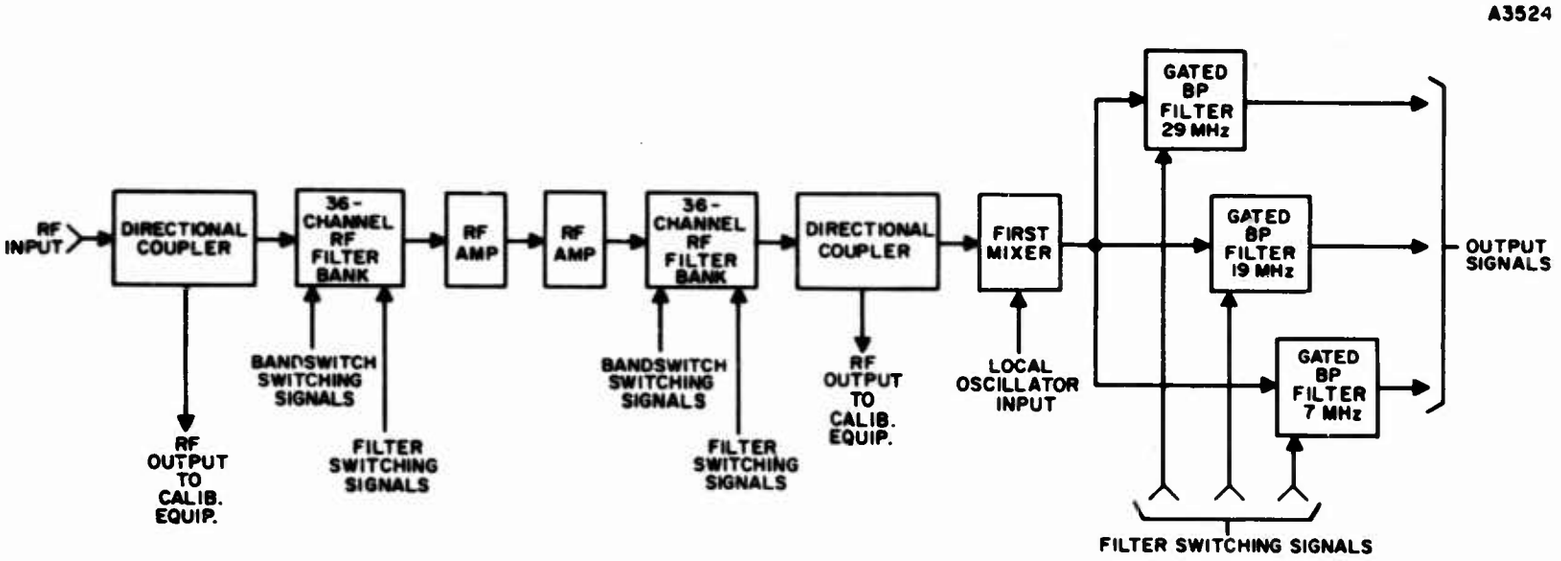


Figure 4. RF Front-End

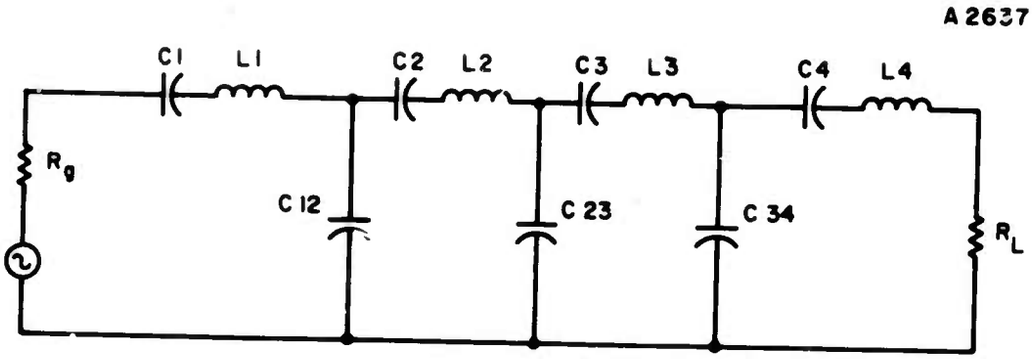


Figure 5. Chosen Bandpass Filter Network Configuration

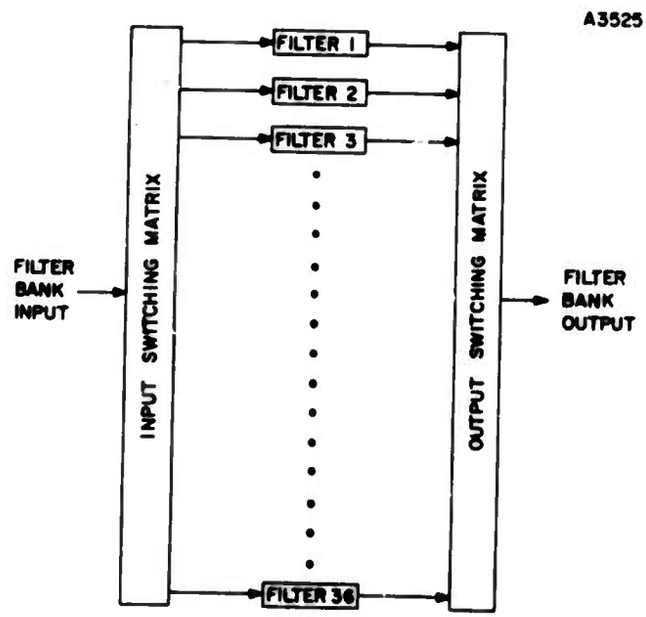


Figure 6. Filter Bank

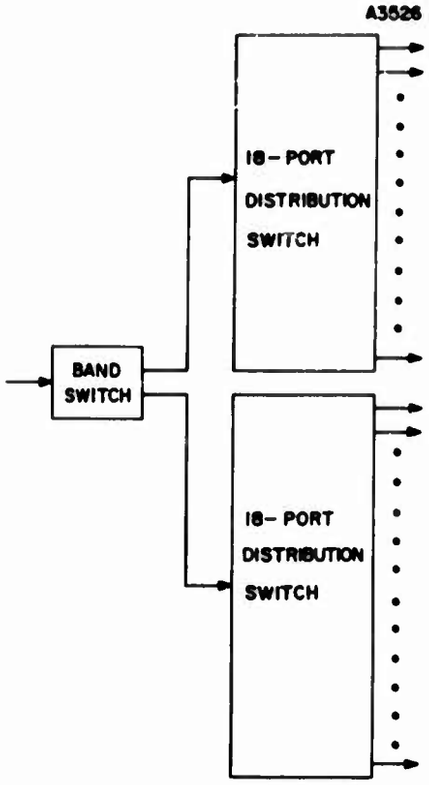


Figure 7. Switching Matrix

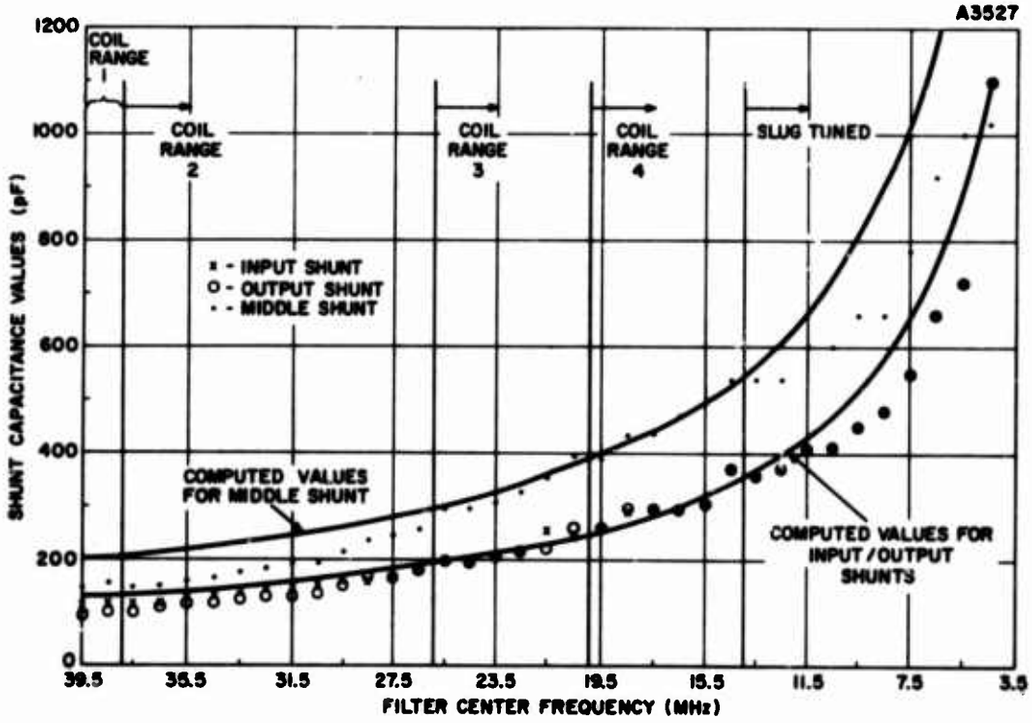


Figure 8. Predicted vs. Actual Shunt Capacitor Valves

approach would result in 35 unterminated coaxial cables loading both the input and output of the activated filter. The final design incorporated the switching at the common node to solve this problem. A block diagram of the switching matrix is shown in Figure 7.

The maximum insertion loss incurred by a signal in traveling through a single RF filter bank was 5.5 dB at 40 MHz; at 4 MHz this loss is approximately 1 dB. These figures include cabling losses of approximately 0.5 dB.

The variation in insertion loss of the filters across the 4- to 40-MHz range was restricted to the 5.5 to 4.0 dB range by using resistive loading on the input and output of the filters (which have inherent loss less than 4.0 dB). This was done to present a constant sensitivity in the low frequency regions where the sensitivity requirements on the receiver are actually less critical, and has the advantage of improving the filter input VSWR characteristic.

Predicted versus actual capacitance values for the three shunt capacitors are shown in Figure 8. The solid curves represent the values as predicted by the design equations, whereas the data points show the nominal values of the capacitors actually used. Five different areas are designated on this graph as COIL RANGE 1, 2, 3, 4 and SLUG TUNED, and represent the frequency range over which a given coil configuration was used. Although the calculated inductance values varied only slightly over the frequency range, the need to vary the coil design was necessitated by the ever-present stray capacitance associated with a given coil. This is illustrated in Figure 9, where the terminal inductance of three different coil designs (as measured by an RX meter) is shown plotted as a function of frequency.

Reasonable agreement between predicted and actual capacitance values is seen in coil ranges 1 and 2, whereas excellent agreement is found in ranges 3 and 4. The discrepancy in the first two ranges is probably due primarily to the impedance reflected to the input of the filters through the coaxial cables by the 18-port distribution switches at the higher frequencies. Notable differences may be observed in the slug-tuned range. These stem primarily from the core losses associated with the tuning slugs.

Since the bandpass characteristics of the filters are of major concern, considerable care was taken in their measurement. The first problem encountered in this area was how to achieve the dynamic range necessary to display filter skirts down to the -60 dB points on an oscilloscope-displayed swept response. This was overcome by using a loga-

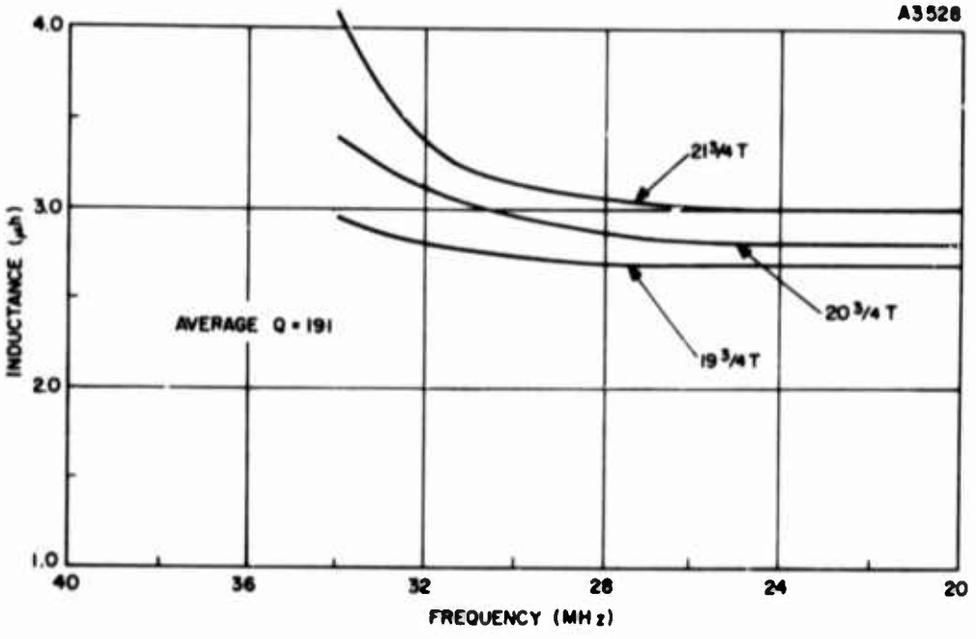


Figure 9. Apparent Coil Inductance

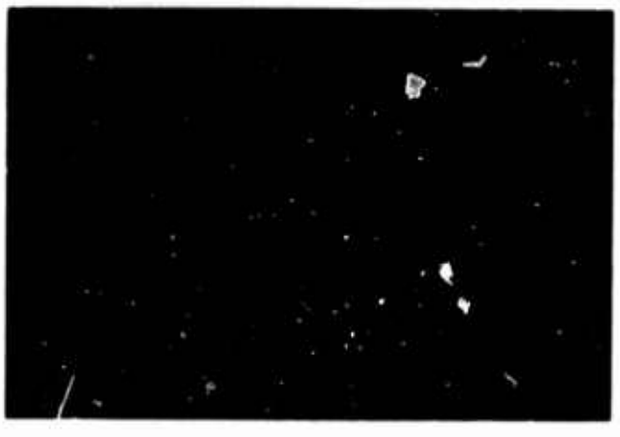


Figure 10. Sweep Rate Effect

Figure 11. 35.9-MHz Filter Skirt Characteristics

rithmic amplifier in the filter output path. The next area of concern was the passband distortion produced by a high sweep deviation index and the relatively high values of filter loaded Q. This problem is graphically illustrated in Figure 10, which shows the results of a high sweep rate on the passband of a 39.5-MHz filter. This picture was produced by sweeping left-to-right and then right-to-left; i.e., the retrace was not blanked. A 60-dB dynamic range is displayed in this photograph. Note the appearance of two apparently different skirts for the same filter. This problem was avoided by using a sweep generator which has a variable sweep rate. The sweep may then be slowed to a point where the frequency modulation produced by the sweeping process does not introduce the high energy sidebands and resultant response distortion.

An indication of the performance achieved in the filters is given in Figures 11 and 12, in which the upper curve is the amplitude response and the lower curve is the VSWR characteristic. Figure 11 shows the skirts on the high frequency side of the 39.5-MHz filter. The total amplitude range of the response is 60 dB; the responses labeled 0 to -50 dB are shown only to calibrate the display. Figure 12 shows the response of the 35.5-, 33.5-, and 31.5-MHz filters (linear display), together with their impedance matching performance. A reference level of 1.3 is indicated for the VSWR since this standard was readily available. These photographs represent the input/output characteristics of the entire filter bank, including the input and output filter switching matrix effects.

The results of filter switching are shown in Figure 13, where the detected output of the filter bank is shown with the 22.5- through 39.5-MHz filters controlled remotely. The amplitude display range is 60 dB.

As mentioned earlier, the method of tuning the filters was changed from capacitive to inductive for the filters centered at 13.5 MHz and below. This change was made for convenience, since the series capacitors in the low frequency filters became so large that the adjustment range of available variable capacitors was insufficient to effect proper tuning. A combination of low required filter loaded-Q and the availability of suitable cores led to the choice of inductive tuning.

Since the isolation of a nonactivated 1-MHz band, as well as the transient performance of the channel switching, is dependent soley on the characteristics of the reed relays used, considerable effort was devoted early in the program to an investigation of these properties for the proposed relay. The results of the isolation measurements are shown in Figure 14, where open-switch attenuation is plotted as a function of frequency. The relay was mounted on a printed circuit board for this test. Data on the settling time of the relays

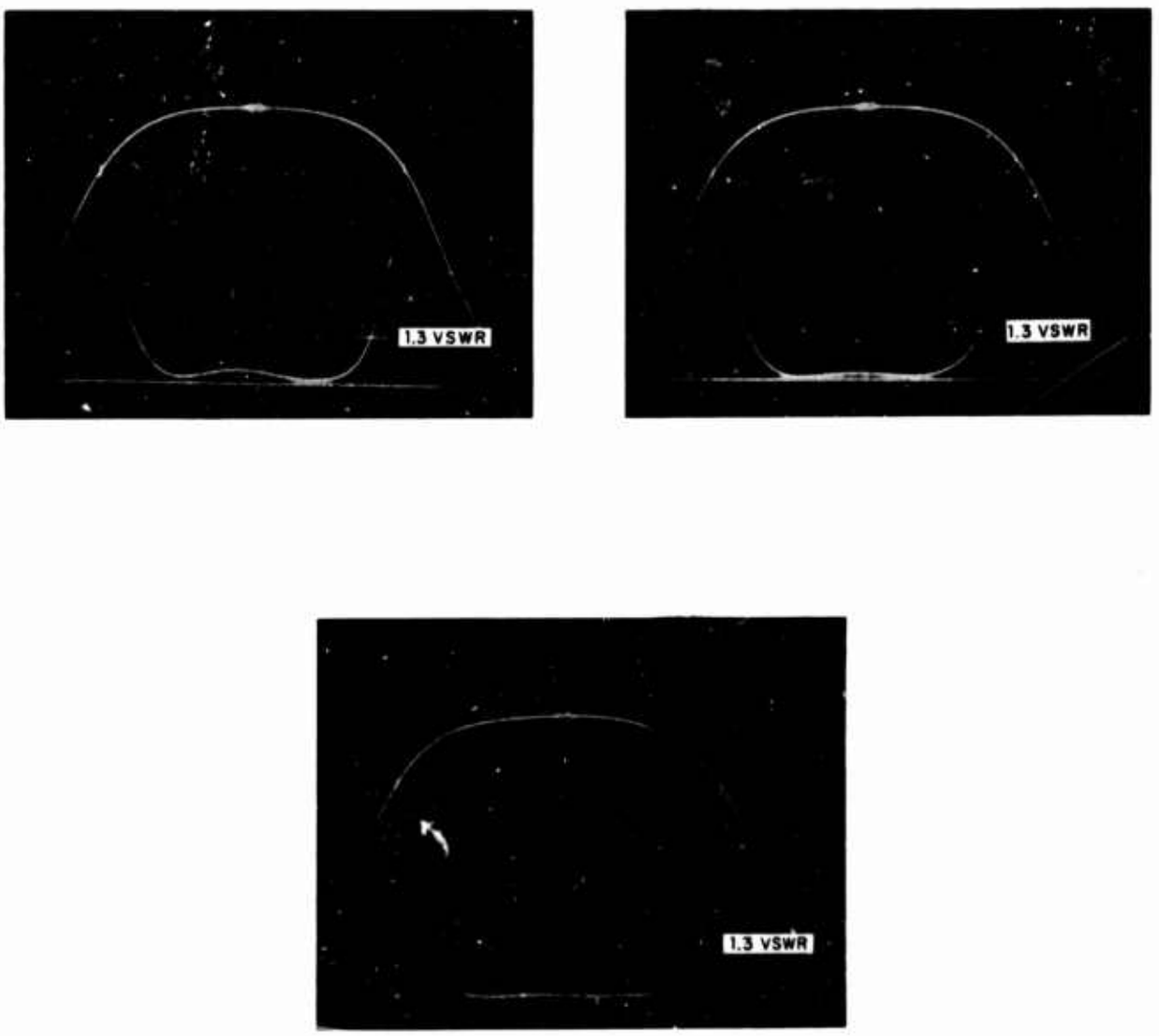


Figure 12. RF Filter Amplitude and VSWR Response

were derived by putting a 40-MHz oscillator at the input to the relay and then activating the relay with a pulse. The output of a typical relay under this test is shown in Figure 15.

The incorporation of the 36 filters and the associated switching into a suitable physical package was a major task. Care was taken so that a standard cable length could be used between the 18-port distribution switching boards and the filters. Separating the switching function into two groups of 18 filters each, with a 2-pole switch to select between the two groups, served to minimize the length of this cable, its associated capacitance, and its insertion loss.

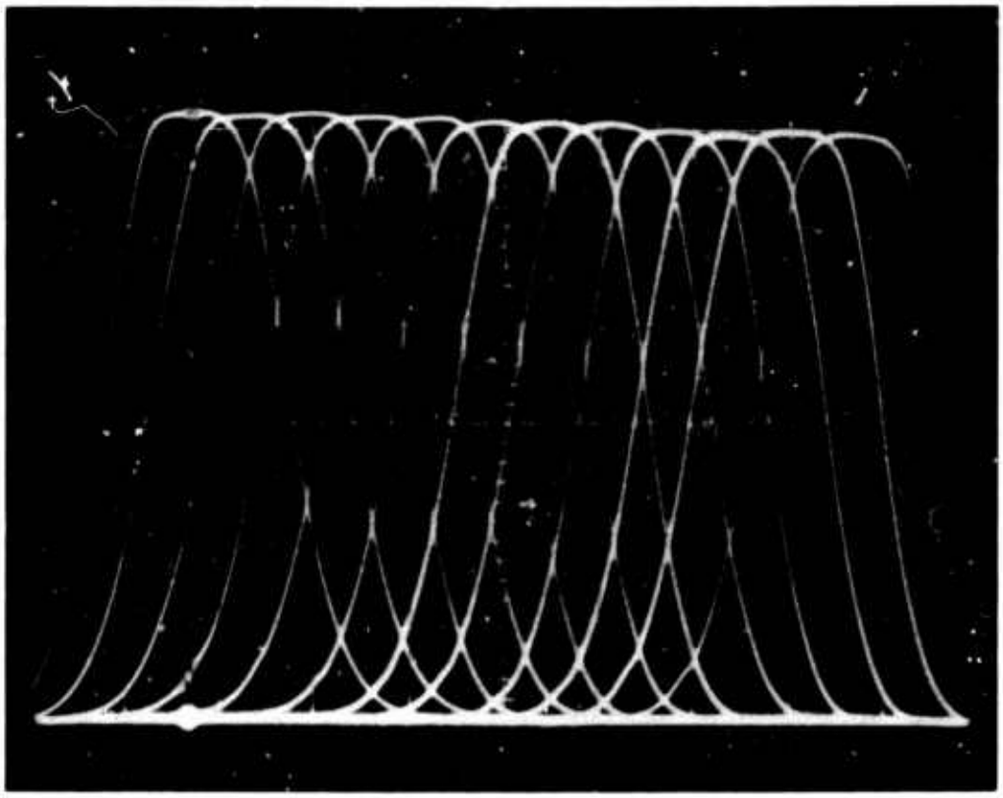


Figure 13. Switched Passband Characteristics

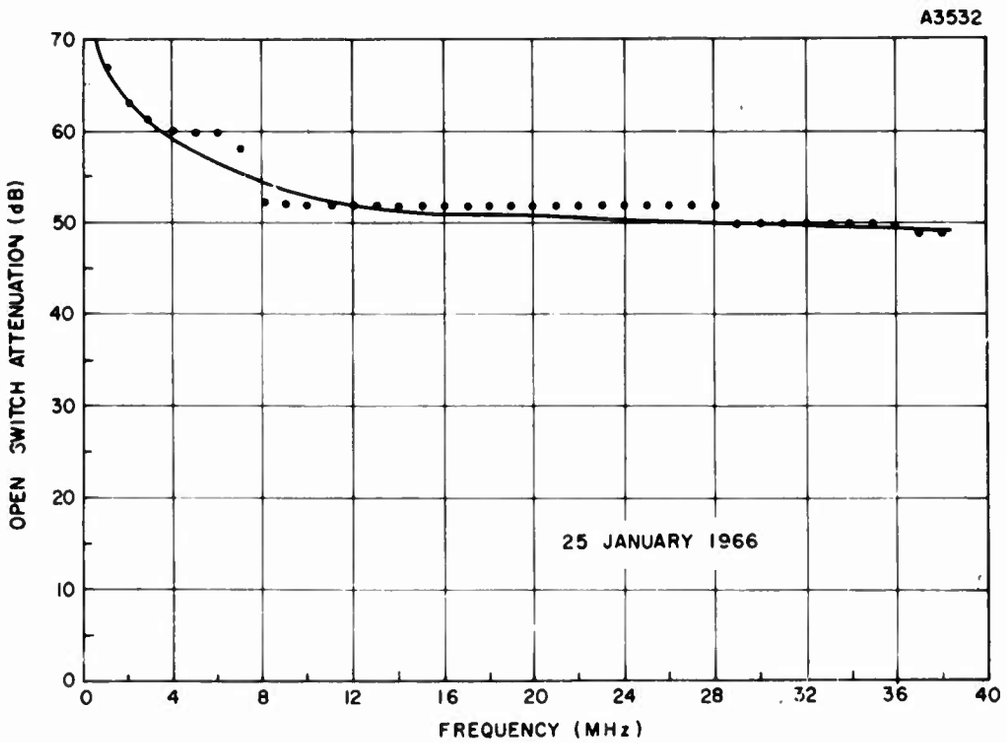


Figure 14. Reed Relay Attenuation

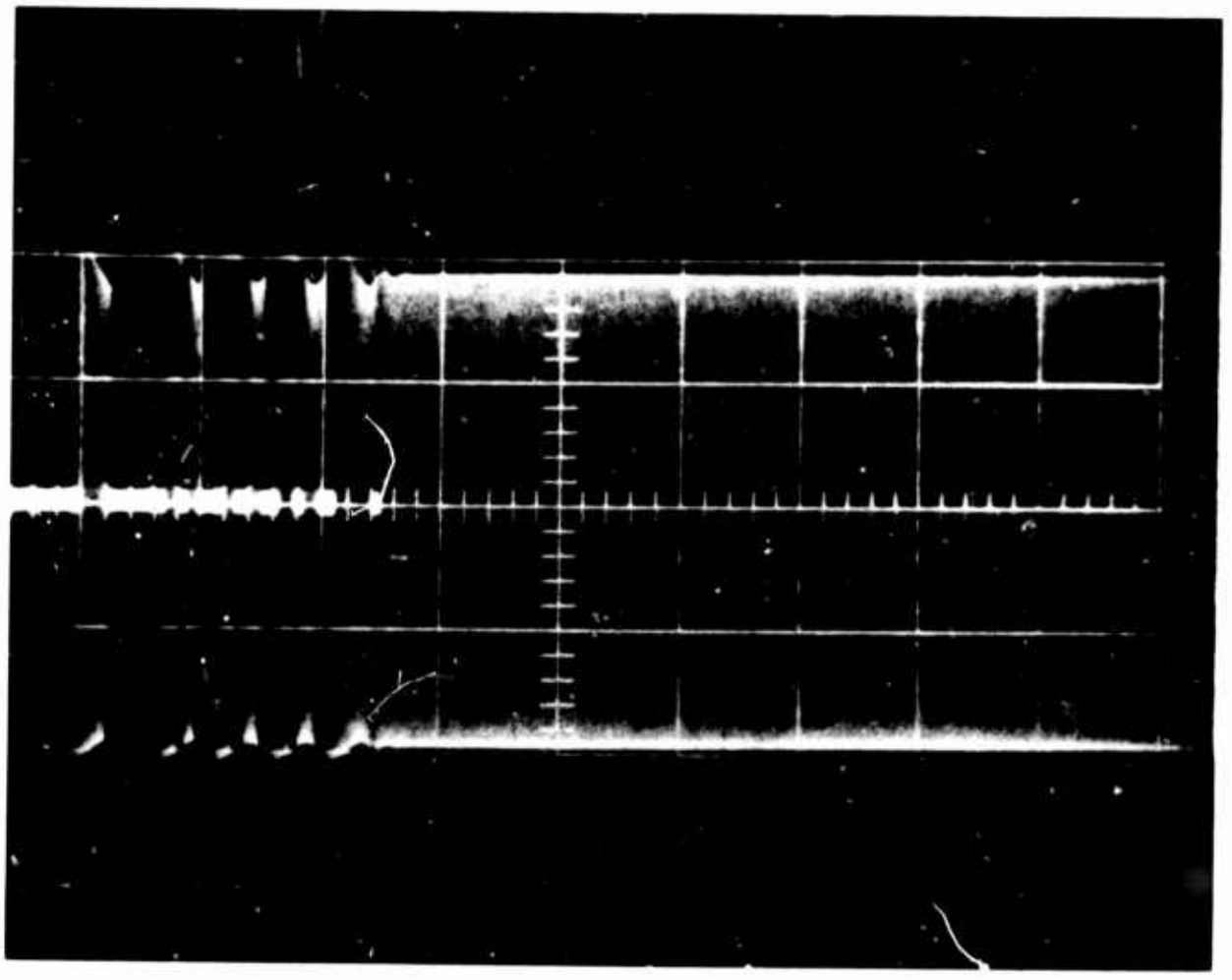


Figure 15. Reed Relay Bounce Characteristics

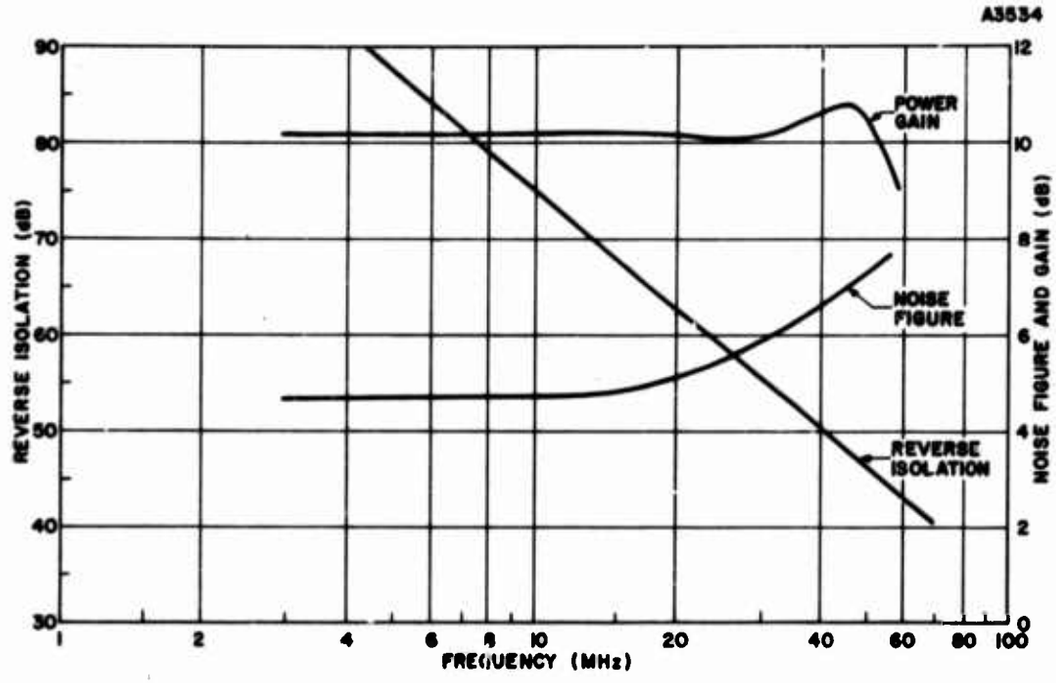


Figure 16. RF Amplifier Characteristics

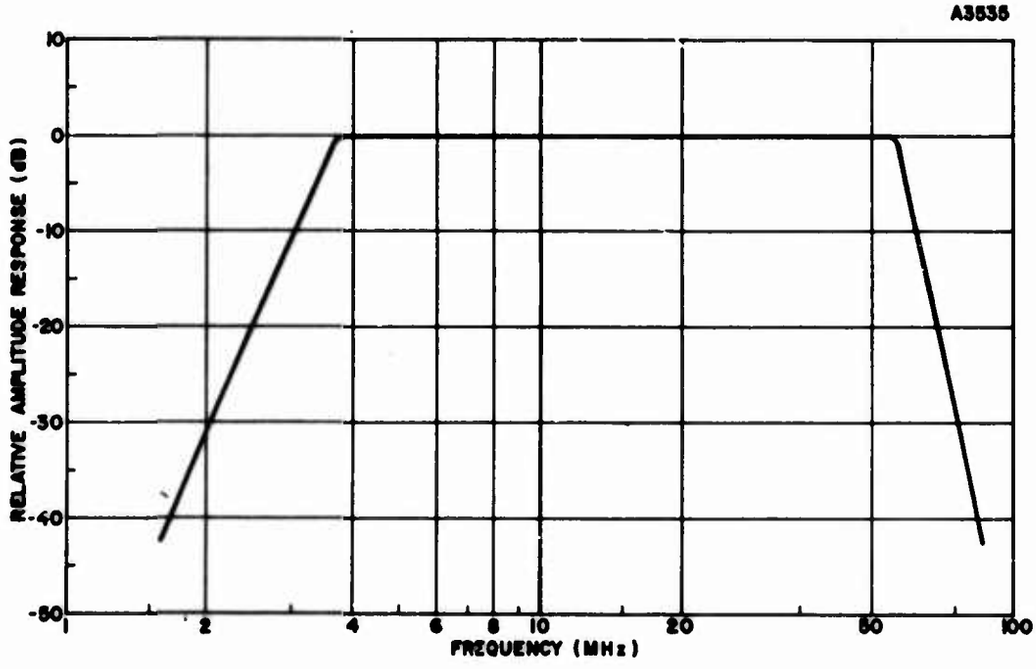


Figure 17. RF Amplifier Amplitude Response

(2) RF Amplifier Design

The RF amplifier for this receiver is a wide-band solid state device designed with special emphasis on highly linear operation. The requirement for a high degree of linearity results from the presence of multiple signals within the 1-MHz preselector filter bandwidth which, if processed by a nonlinear amplifying device, could give rise to in-band cross-products which cannot be distinguished from the desired signals. Salient specifications for the RF amplifier are given in Table II.

TABLE II

RF AMPLIFIER SPECIFICATIONS

Amplitude response over 4- to 40-MHz range	Flat to within ±0.5 dB maximum
Input and output impedance level	50 Ω nominal
Insertion gain	10 dB minimum
Intermodulation distortion products produced by two 50-mv rms in-band input signals as measured at amplifier output terminals	-90 dB maximum
Terminal noise figure	8 dB maximum
Isolation between input and output terminals	40 dB minimum
Device complement	All solid state

The device which has been selected to perform this function in the receiver is a modified version of a standard model multicoupler produced by the TRG Division of the Control Data Corporation. Modifications to the standard unit consisted primarily of widening the amplifier bandwidth. This amplifier achieves the required low intermodulation distortion levels by the use of transistors intended primarily for application in high frequency power amplifiers. Several such devices are employed in order to achieve high open-loop gain. Negative feedback is then employed to trade off the excess gain in order to reduce distortion and widen the amplifier bandwidth.

Figures 16 and 17 show the behavior of power gain, noise figure, reverse isolation, and input filter amplitude response versus frequency for a typical RF amplifier. Variations in power gain and noise figure between units operating at the same frequency are almost nonexistent, reflecting the use of large amounts of negative feedback. Table III shows typical intermodulation distortion data resulting from the application of two 50-mv rms signals at the indicated frequencies.

TABLE III

INTERMODULATION DISTORTION PERFORMANCE

Signal Generator Frequency (MHz)	Signal Generator Frequency (MHz)	Intermodulation Distortion Product Frequency (MHz) and Amplitude (dB)					
f_1	f_2	$f_1 - f_2$	$f_1 + f_2$	$2f_1 - f_2$	$2f_1 + f_2$	$2f_2 - f_1$	$2f_2 + f_1$
8	5.6	2.4	13.6	10.4	21.6	3.2	19.2 MHz
		*	90	97	106	*	102 dB
30	21	9.0	51	39	81	12	72 MHz
		91	*	103	*	104	* dB
50	35	15	85	65	135	20	120 MHz
		90	*	*	*	92	* dB

*Product frequencies lie outside band of interest.

(3) First Mixer Design

The performance requirements for the first mixer stage of the receiver, in general, parallel those of the RF amplifier. A high degree of linearity is required again to avoid the creation of cross-products resulting from the presence of multiple high amplitude in-band signals at the mixer input port. Obviously, the lowest possible noise figure is also required for good receiver sensitivity.

These requirements are even more difficult to attain in a high frequency mixer than in an amplifier, since for the amplifier, the fundamental frequency term represents the desired output; the design problem then is one of optimizing the first-power or fundamental frequency term of the power series which expresses the transfer characteristic of the stage, at the expense of all other terms. In cases where highly linear operation is required and bipolar transistors are employed as the active device, the common-base configuration is often employed to perform this optimization. In the mixer, however, the desired term is the square-law term and the problem now is one of optimizing the second-power term at the expense of all other terms. In other words, nonlinear operation of a very restrictive nature is required for good mixer performance.

The specifications to which the first mixer stage was designed are listed in Table IV.

TABLE IV

FIRST MIXER SPECIFICATIONS

Noise figure	9 dB maximum
Conversion loss	8 dB nominal
Conversion loss variation across 4- to 40-MHz band	±1 dB
Input and output impedance level	50Ω nominal
Intermodulation distortion products produced by two 120-mv rms in-band signals as measured at mixer output terminals	-75 dB nominal
Device complement	Solid state

Work performed on a mixer investigation with similar requirements indicated that although new devices, such as the insulated-gate field effect transistor, show promise for the future, the best mixer device currently available to the circuit designer is still the diode.

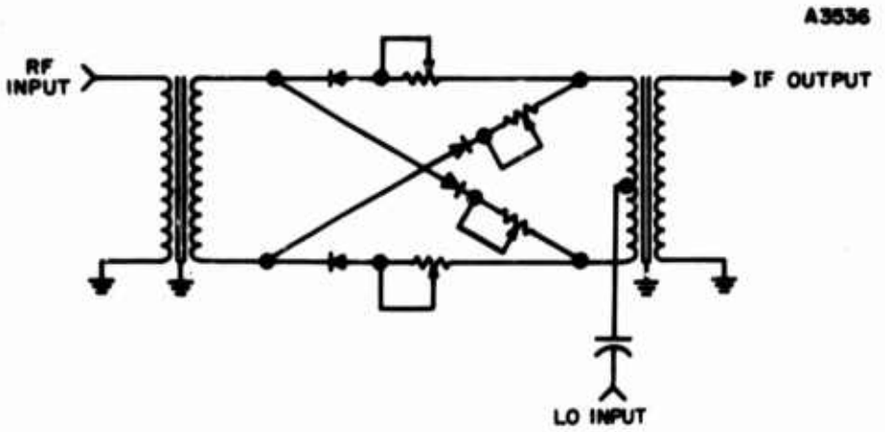


Figure 18. First Mixer Stage

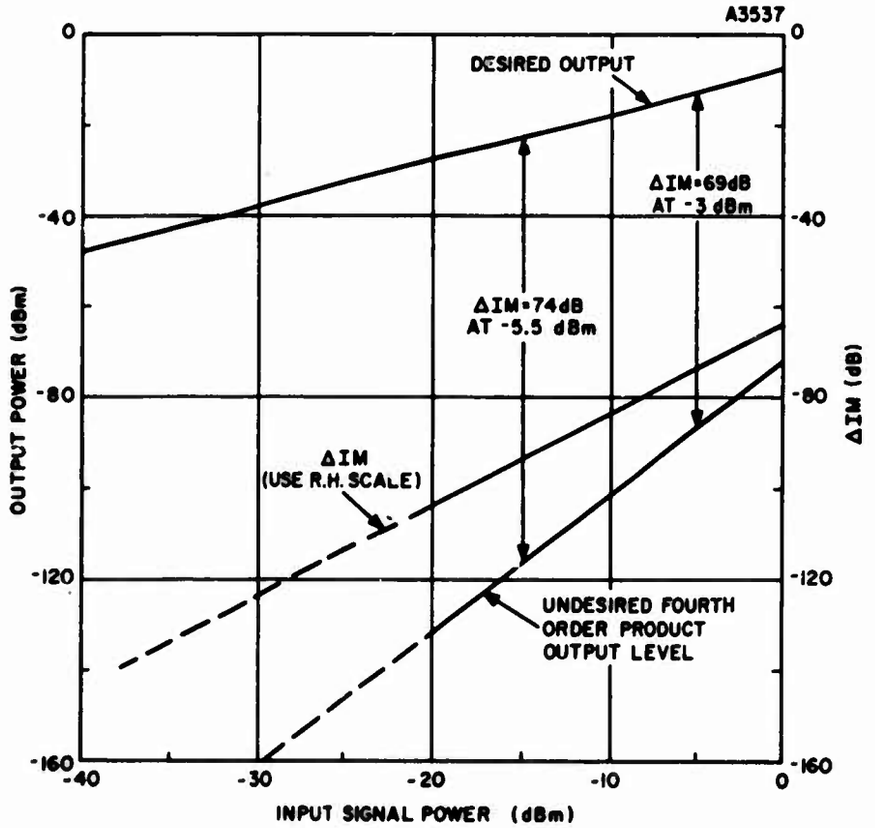


Figure 19. First Mixer Intermodulation Distortion Performance

Figure 18 is the circuit diagram of the first mixer stage. Hot-carrier diodes are employed in this design, primarily because their lower excess noise contribution provides a slight improvement in noise figure performance. The novel feature of this circuit is its use of balancing resistors, not primarily to promote good signal or local oscillator balance, but to improve intermodulation distortion (IM) performance. While it is true that the use of large amounts (i.e., greater than 1000 ohms) of resistance in series with each diode in a diode mixer will always improve mixer distortion performance, this improvement can only be obtained at a considerable sacrifice in noise figure performance. In the design employed here, however, the sacrifice in noise figure performance is very modest (i.e., 2 to 3 dB), while the improvement in distortion performance can be made to approach 30 dB at large input signal levels.

Figure 19 illustrates the IM distortion performance of the first mixer stage described above at 4.5 MHz; IM performance at 40 MHz degrades approximately 10 dB. Conversion loss is typically 8 dB at 4 MHz and 8.5 dB at 40 MHz.

(4) Gated IF Filter Design

The 29-, 19-, and 7-MHz filters employed to filter the IF output signals from the first mixer are identical in design to those employed in the RF filter banks at 29.5, 19.5, and 7.5 MHz, respectively, except for the addition of a reed switch which performs the gating function. The adjustment range of the tunable filter components is substantially in excess of that necessary to shift the filter center frequency the required 0.5 MHz.

b. IF Amplifier Unit

The IF amplifier unit accepts signals from the receiver front-end unit, amplifies and filters them at one of the three first IF's, and converts the signal frequency in a second mixing step to 3 MHz, where final filtering, amplification, detection, and integration are accomplished.

Three second IF amplifier paths are employed to process the 120-dB receiver input signal amplitude range for which the noise interference receiver is designed, since the dynamic range of the detector stage is limited to approximately 40 dB for reasonable values of IF signal power at the detector input terminals. Since the total gain in each of these three parallel paths differs by the same 40-dB figure, then as long as the receiver input signal falls within the prescribed 120-dB amplitude range, one of the three detectors will always be handling a signal within its prescribed 40-dB IF signal amplitude range, while the other two detectors are either saturated or producing no output.

A second IF bandwidth of 4 kHz is provided for those measurements employing the 0.3- and 3-second integration periods. In addition, a 1-kHz bandwidth is available for use exclusively with the 500-second integration period. The latter feature has been incorporated to allow data to be recorded under similar conditions to those employed by CCIR in their worldwide noise monitoring activities.

(1) First IF Amplifier Design

The configuration of the first IF amplifier is basically unchanged from the breadboard circuit described in Interim Report No. 1. In order to provide for better gain and input matching, a pi-network has been added to the amplifier and a gain control has been provided for each of the two 10-dB gain sections of this amplifier.

The electrical performance attained in each 10-dB gain section of the amplifier is delineated in Table V.

TABLE V

IF AMPLIFIER PERFORMANCE

Amplifier gain	14.5 dB
Noise figure	9 dB maximum
Input impedance	50 ohms
Output impedance	50 ohms
Amplifier input VSWR	1.05 maximum
Amplifier output VSWR	1.05 maximum
Intermodulation product levels at amplifier output terminals resulting from two in-RF-band 33-mv signals at the 50-ohm input terminals	-75 dB

All three amplifiers at the three intermediate frequencies of 7, 19, and 29 MHz are capable of the performance listed above.

As shown in Figure 20, the IF amplifier consists of two identical sections separated by a narrow-band filter. Filter performance requirements are shown in Table VI.

TABLE VI

FILTER PERFORMANCE REQUIREMENTS

Bandwidth (-3 dB)	5.6 kHz
Shape factor (6/30 dB)	3 maximum at 7 MHz 3 maximum at 19 MHz 4.5 maximum at 29 MHz
In-band ripple	±0.4 dB
Insertion loss	3.5 dB maximum
Nominal source and load impedance	50 ohms

Figure 21 shows the amplitude response curves of the three filters employed in the first IF amplifier. Figure 22 is a schematic of the final amplifier configuration showing both amplifiers and the narrow-band crystal filter in series. Of the several transistors employed, the 2N3137 gave the best combination of intermodulation performance, noise figure, and gain. Figure 23 is a photograph of the final amplifier board.

(2) Second Mixer Design

The second mixer stage is identical in design to the first mixer, except that a reed switch in series with the mixer output has been added to accomplish the necessary gating. This insures that only one signal path to the second IF amplifier stages exists at a given time.

(3) Second IF Amplifier Design

The second IF amplifier consists of a preamplifier, a bandpass filter, a four-way power divider, and three parallel amplitude channels (Figure 24).

The preamplifier and the amplifiers which follow the power divider are of identical design, with the exception that the amplifiers which drive the detector/integrator stages do not contain an output attenuator.

The design specifications for this amplifier are given in Table VII.

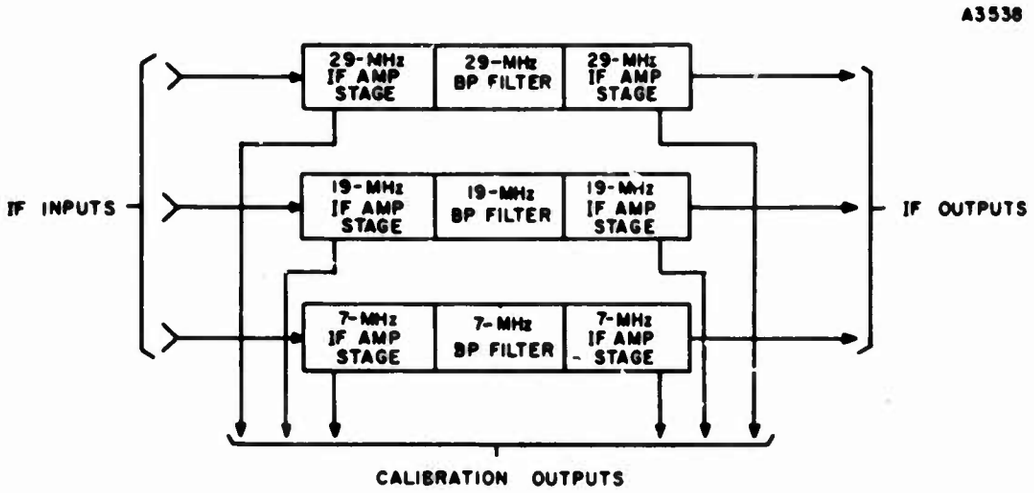


Figure 20. First IF Amplifier, Block Diagram

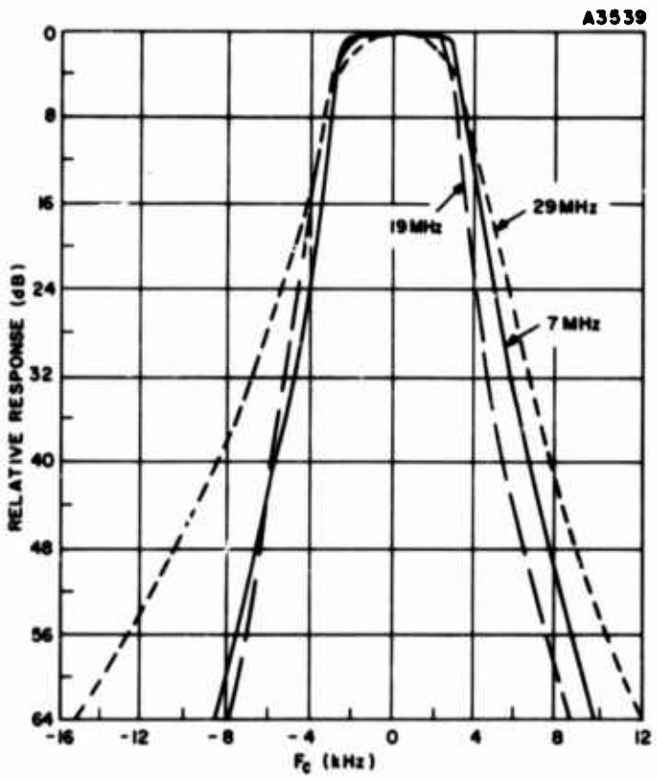


Figure 21. First IF Amplifier, Amplitude Response

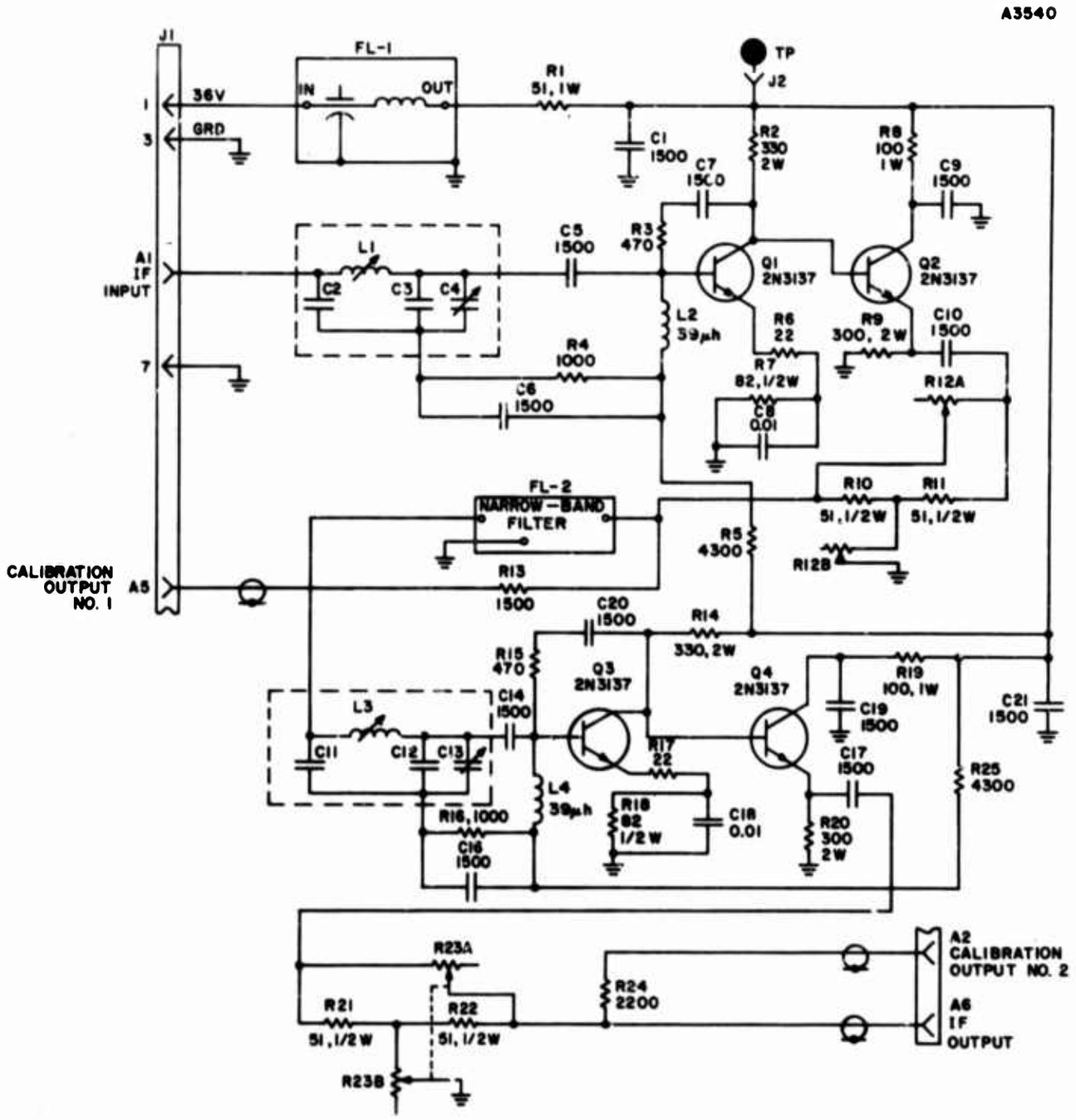


Figure 22. First IF Amplifier, Schematic Diagram

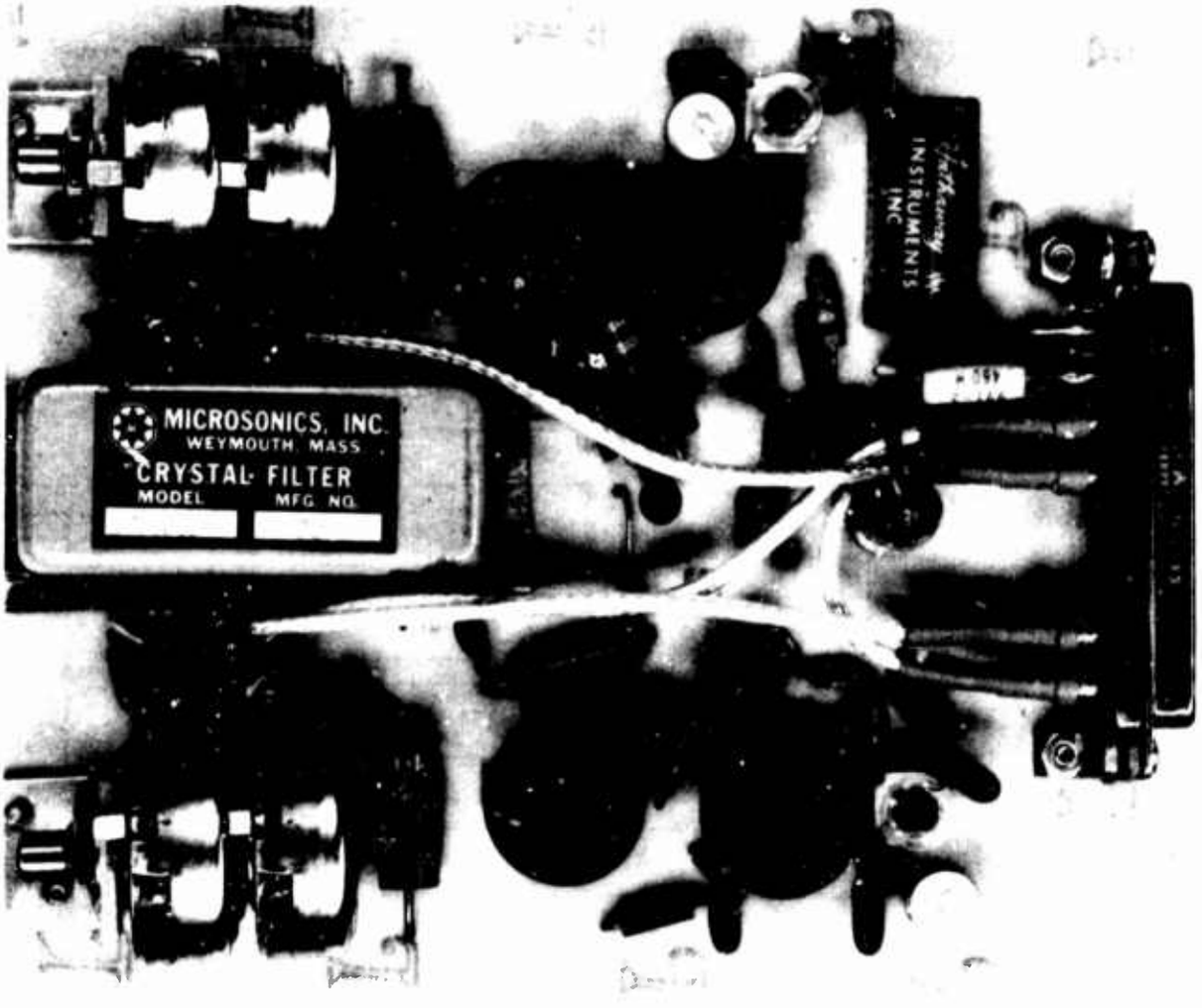


Figure 23. First IF Amplifier Board

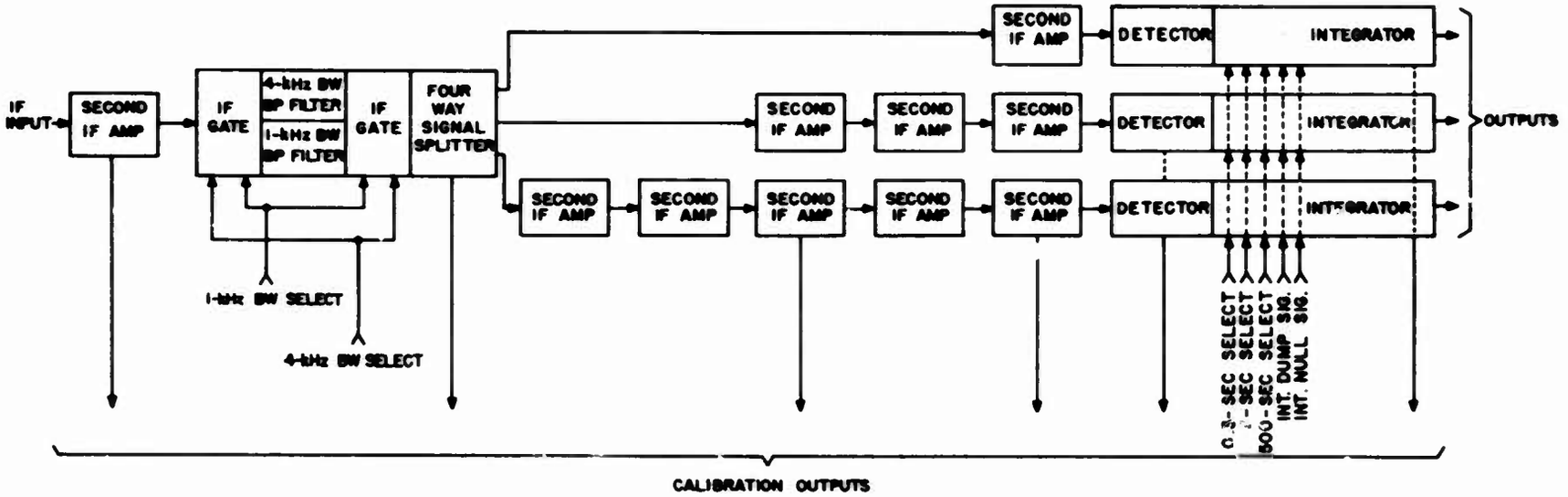


Figure 24. Second IF Amplifier, Block Diagram

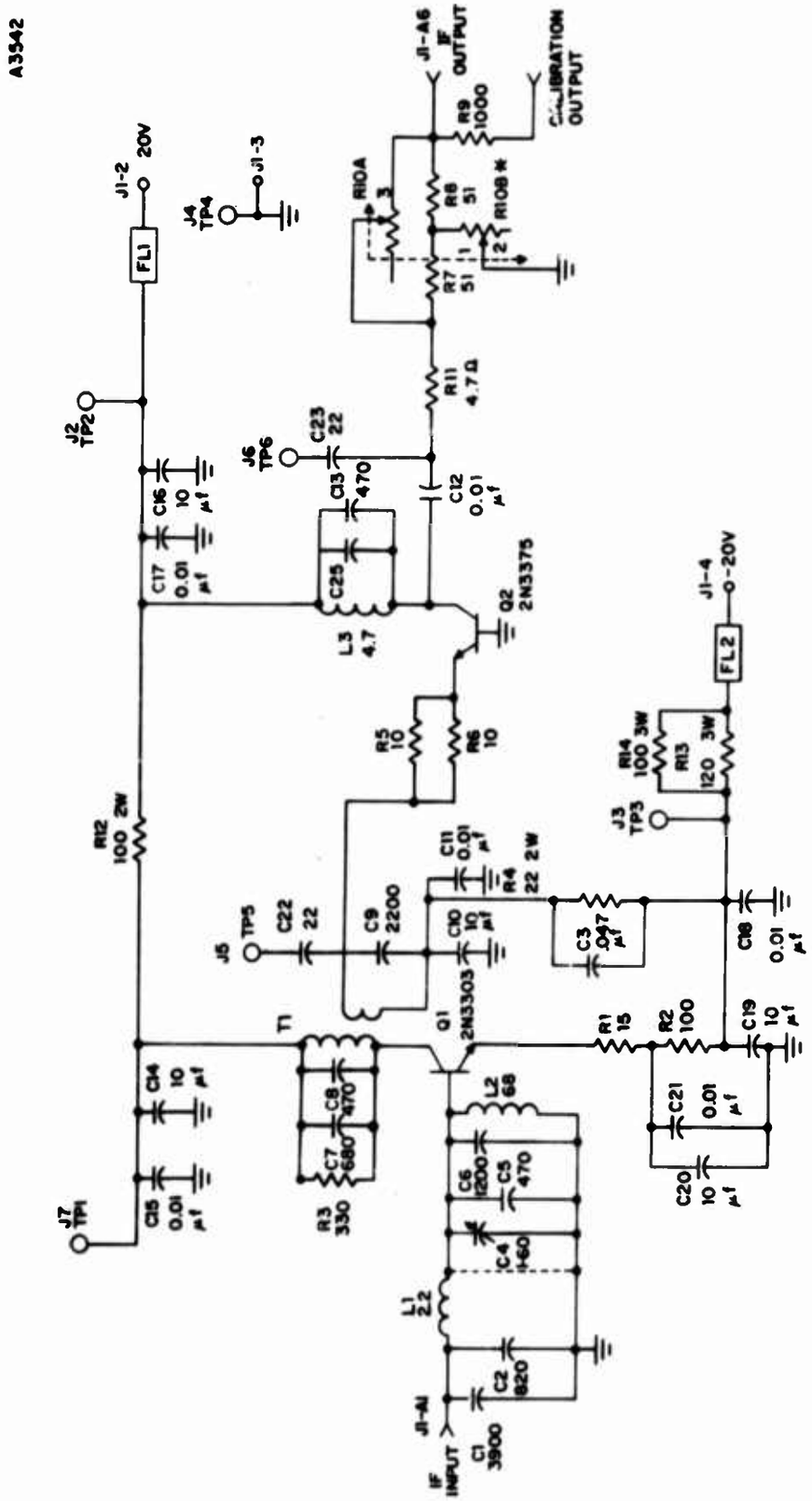


Figure 25. Second IF Amplifier, Schematic

TABLE VII

SECOND IF AMPLIFIER SPECIFICATIONS

Center frequency	3.0 MHz
Gain	26 dB (6 dB variable)
Input impedance	50 ohms
Nominal bandwidth (3 dB)	300 kHz
Noise figure	6 dB maximum
IM product levels:	
Two 158-mv rms input signals, both in-band	40 dB maximum
One in-band and one out-of-band signal, both 158-mv rms at amplifier input	90 dB maximum

A pi-network with capacitive shunt arms and an inductive series arm is employed for matching the 50-ohm source impedance to the first stage (Figure 25). The design equations for this network are as follows:

$$X_A = \frac{-R_1 X_B}{R_1 \pm \sqrt{R_1 R_2 - X_B^2}} \quad (1)$$

$$X_B = \frac{-R_2 X_B}{R_2 \pm \sqrt{R_1 R_2 - X_B^2}} \quad (2)$$

where

$$X_B = R_1 R_2 \quad (3)$$

R_1 = source impedance = 50 ohms

R_2 = transistor input impedance

X_A = capacitive reactance at source

X_B = inductive reactance of series arm

X_C = capacitive reactance at load

The measured transistor input impedance was 410 ohms.

$$\sqrt{R_1 R_2} = \sqrt{(50)\ (410)} = 145 \text{ ohms}$$

Choose $|X_b|$ = 42 ohms

L_b = 2.2 μh

Then, from Equations (1) and (2),

X_A = -11.3 ohms and C_A = 4600 pf

X_C = -31.4 ohms and C_C = 1700 pf

These calculated values are, of course, approximate and required some adjustment to compensate for parasitics and component tolerances. Using the component values shown in Figure 25, the input VSWR ranged from 1.1 to 1.2 for 24 production units.

The first amplifier stage was of prime importance in determining the overall noise figure and the third-order intermodulation product, both of which are directly affected by the quiescent collector current. Generally, increasing collector current degrades noise figure performance while IM performance is improved. Measurement of noise figure and IM products at several values of collector current resulted in the selection of 50 ma as the best compromise.

The 2N3375 output transistor is used in the common-base configuration in order to obtain linear operation over a wider range of collector current at the high signal levels.

Results of tests on 24 production units are shown in Table VIII.

TABLE VIII

SECOND IF AMPLIFIER TEST RESULTS

Parameter	Range of Readings Recorded	Mean Value
Noise figure	6.0 to 7.4 dB	6.5 dB
Gain (maximum)	25.4 to 27.4 dB	26.5 dB
Bandwidth (-3 dB)	300 to 340 kHz	315 kHz
VSWR	1.1 to 1.2	1.15
IM product level at V_{out} = 3.2 v rms at 50 ohms	-28 to -35 dB	-30 dB

(4) Detector Integrator Design

The detector integrator assembly receives 3-MHz signals from the second IF amplifier. The detector is required to operate linearly within ±1 dB for a 40-dB input signal range. The integrator which follows is therefore required to integrate linearly for a 40-dB signal range, providing an output voltage that varies between 0.1 and 10 v dc. The integrator

load current at 10 v dc output may not exceed 2 ma. Three selectable integration periods are provided (0.3, 3, and 500 seconds) and are selected by applying 12 v dc to one of the three control relays.

In order for the detector to achieve a 40-dB linear range, three special circuit precautions have been observed: (1) the detector diode is slightly forward-biased in its quiescent state, (2) the diode is driven from a high impedance source by use of a transformer to match the 50-ohm second IF amplifier output impedance to the 10K detector load, and (3) the detector is driven from a common-base stage. The common-base driver stage helps to extend the linear operating region tc a lower input signal level, since, as the input drops, the detector diodes present a higher load impedance to the driver, thus increasing the driver output voltage. This increase tends to compensate for the increasing diode resistance. An adjustable voltage translating network, employing two potentiometers, is used to scale the detector output voltage range to the optimum range for the integrator which follows.

The 500-second integration time requirement plus the 40-dB input range requirement resulted in choosing the operational amplifier type of integrator. In order to better understand the problems involved in the above requirement, an operational amplifier integrator design will be reviewed. Referring to Figure 26, it is seen that

$$e_o = -K\, e_g \tag{4}$$

or, rearranging

$$e_g = -\frac{e_o}{K}$$

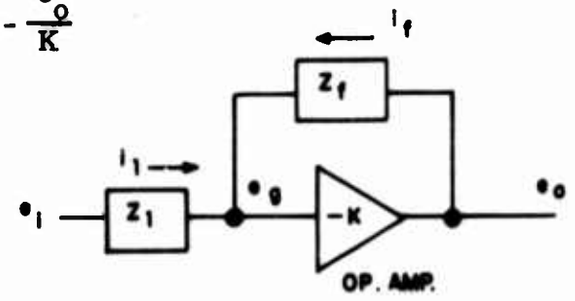


Figure 26. Feedback Circuit Using an Operational Amplifier

It is also seen that

$$i_1 = \frac{e_1 - e_g}{Z_1} \tag{5}$$

and

$$i_f = \frac{e_o - e_g}{Z_f} \tag{6}$$

In the ideal operational amplifier

$$i_1 + i_f = 0 \tag{7}$$

Substituting Equations (5) and (6) into Equation (7) results in

$$\frac{e_1 - e_g}{Z_1} + \frac{e_o - e_g}{Z_f} = 0 \tag{8}$$

With the further substitution of Equation (4) into Equation (8) the result is

$$\frac{e_1}{Z_1} = \frac{-e_o}{Z_f}\left(1 + \frac{1}{K} + \frac{Z_f}{KZ_1}\right) \tag{9}$$

In the ideal operational amplifier the amplification, K, is infinity, so that

$$\frac{e_o}{e_1} = \frac{-Z_f}{Z_1} \tag{10}$$

When Z_f is the impedance of a capacitor and Z_1 is the impedance of a resistor, using the Laplace transform,

$$Z_f = \frac{1}{sC_f} \tag{11}$$

$$Z_1 = R_1 \tag{12}$$

Substituting for Z_f and Z_1 in Equation (10) results in

$$\frac{E_o}{E_i}(s) = \frac{-1}{sR_1C_f} \tag{13}$$

which is the transfer function of an integrator.

When $E_1(s)$ is a step function, $E_1(s) = \frac{E}{s}$ and Equation (13) becomes

$$E_o(s) = \frac{-E}{s^2R_1C_f} \tag{14}$$

or

$$e_o = \frac{-E}{R_1C_f}t \tag{15}$$

in the time domain. The output for a step function input is shown in Figure 27.

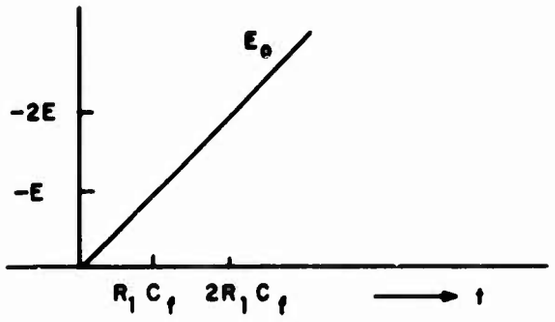


Figure 27. Integrator Output for a Step Function Input

The maximum output voltage requirement, E_o = 10 v, may be substituted into Equation (15) to find the required E_{in} (max) for 500 seconds of integration as follows.

$$E_{in}\,(max) = \frac{E_o\,(max)(R_1 C_f)}{t} + \frac{10\,R_1\,C_f}{500} = 2R_1 C_f \times 10^{-2} \qquad (16)$$

Then E_{in} (min) will equal $2R_1 C_f \times 10^{-4}$. The minimum input current will then be

$$\frac{E_{in}(min)}{R_1} = \frac{2R_1 C_f \times 10^{-4}}{R_1} = 2C_f \times 10^{-4}$$

With C_f = 10 μf the minimum input current equals 2 na.

A 10-μf polystyrene capacitor has an approximate resistance of 100,000 megohms. Then the leakage current, when the output is 10 v, would be 1×10^{-10} ampere. A mylar capacitor with an approximate resistance of 10,000 megohms would have a leakage current of 1×10^{-9} ampere when the output is 10 v. These are the maximum leakages which can occur.

Capacitor leakage current allows the signal input current to bypass the amplifier causing error; for instance, if the capacitor leakage current equaled the signal input current, no current would enter the amplifier and no change in output (no integration) would occur. This would result in 100 percent error in integration during this time. The error caused by leakage current equals $\frac{\text{capacitor leakage current}}{\text{signal input current}} \times 100$ percent. The worst error caused by leakage current will occur when the output voltage is maximum (causing the greatest capacitor leakage current) and the signal input current is at the same time at its smallest value. Using a mylar capacitor, when the output is 10 v and the signal input current is 2 na, the maximum possible error caused by leakage current is 50 percent. This error can be reduced to five percent by using a polystyrene capacitor; however, because of the large physical size of the polystyrene capacitor, mylar capacitors were used in the circuits for this receiver.

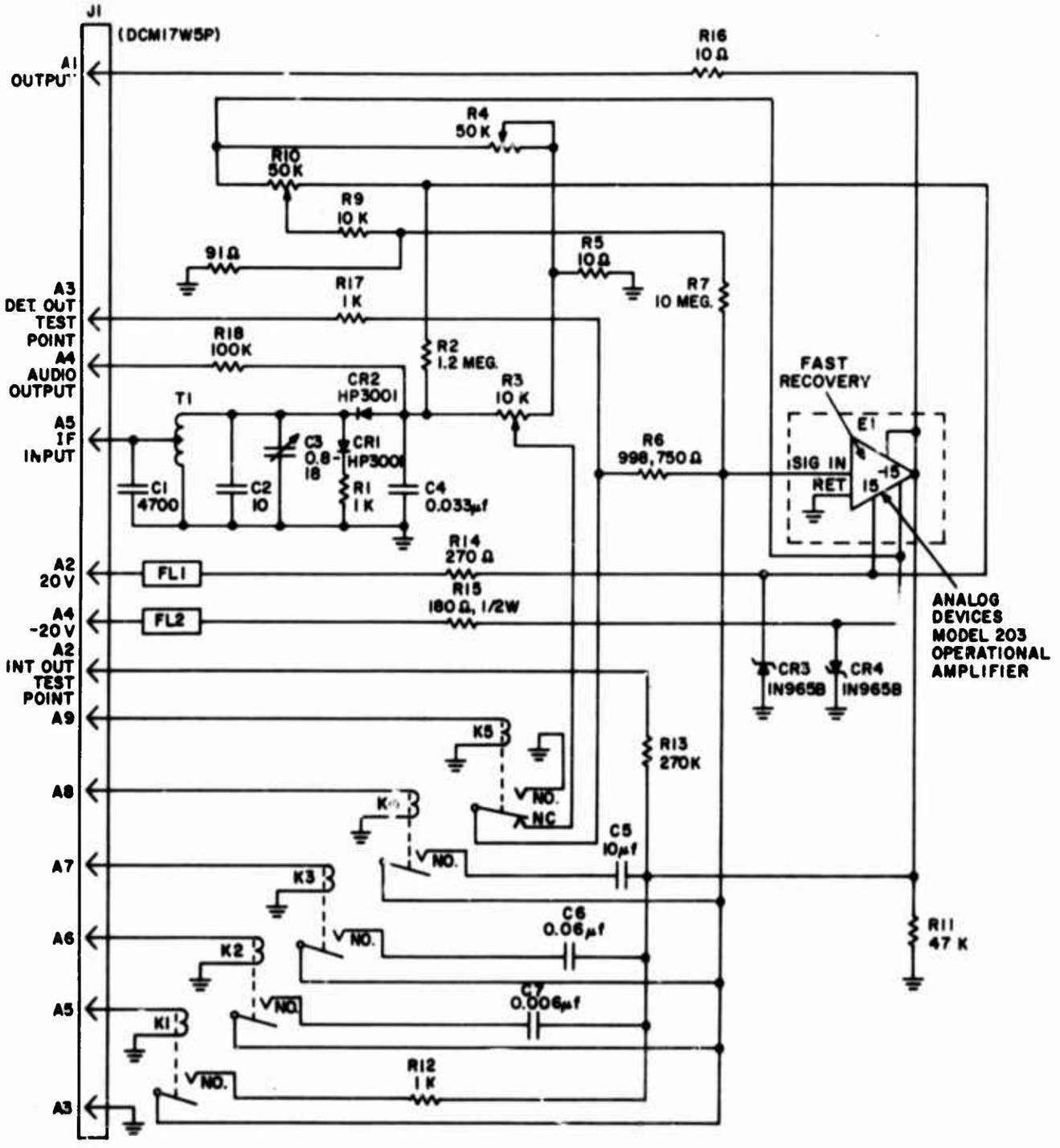


Figure 28. Detector/Integrator

Another error to be considered in the design of the integrator is that due to R_1 and C_f. Since the output voltage, E_o, is proportional to R_1C_f, any error in the value of these components contributes directly to percent of error in the output. For this reason, 0.5 percent capacitors and a 0.1-percent resistor with a temperature coefficient of 10 ppm/°C and good long term stability (0.003 percent/year) are used.

Any amount of drift in the amplifier during the integration time will result in an error in the integrated output. The situation is alleviated somewhat in that the output of the integrator is dumped after each integration period; thus, for a short period (such as 0.3 second), the drift of the amplifier normally presents no problem. For the 500-second integration period, however, the drift could be significant. In some cases, a resistor network may be used to feed back a small amount of signal from the output to reduce the drift; however, as shown above even 10,000 megohms of feedback resistance can cause a 50 percent error when the minimum signal is being received. Therefore, the problem has been resolved by a low drift (0.2 μv/°C) operational amplifier, with a potentiometer employed to set the drift to a minimum. With the minimum input signal level this particular drift component will contribute a less than 10 percent error during the 500-second integration time.

The operational amplifier is prevented from saturating by a self-contained zener diode network, so that recovery from full output requires less than 0.5 μs.

A schematic diagram of the integrator/detector is shown in Figure 28.

c. Receiver Calibration Unit

Due to the nature of the HF propagation medium, it is necessary to gather large amounts of data if statistical estimates of HF noise level and interfering signal amplitudes are to be derived with high confidence. In an effort to assure the accuracy of the data gathered by the noise interference receiver, and to assure equipment availability by decreasing downtime due to failures, an extensive self-checking capability has been built into the receiver. The self-contained test equipment and switching required to perform this task compose the receiver calibration unit, for which component equipments are described in detail below.

(1) RF Signal Generator

The signal used to calibrate the receiver is generated by a Hewlett Packard 606AR HF signal generator. This device covers the required 4- to 40-MHz range in three continuously variable bands. A feedback circuit makes it unnecessary to readjust the output level when varying frequency over the entire range.

A frequency calibrator crystal oscillator provides accurate check points every 100 kHz up to 6 MHz and every 1 MHz above 6 MHz. While the frequency of the instrument itself has a ± 1 percent accuracy, the calibrator is accurate to within 0.01 percent, making it ideal as the source of a receiver calibration signal. Its rated frequency stability is 50×10^{-6}, or 50 Hz per MHz for any 10-minute period.

A hybrid junction is employed at the signal generator output port to furnish calibration signals to both receiver channels simultaneously.

(2) Voltmeter Switching Assembly

Eighteen RF and IF points in each of the two receiver channels are monitored by means of separate calibration outputs provided in addition to normal signal outputs. These signals are connected through relay networks to the RF calibration voltmeter by the voltmeter switching assembly. Rotary switches on the front panel of this assembly permit the selection of any one of the outputs by energizing the proper relay.

A series resistive divider network has been placed in each calibration signal circuit so that each calibration signal may be adjusted to the same value (approximately 5 mv). This facilitates rapid checking of the relatively large number of calibration signal levels, since the voltmeter range switch need not be changed for each measurement; and, in fact, the meter needle should indicate essentially the same midscale reading until an out-of-spec reading is encountered.

Each of the receiver's six detectors and six integrators have similar calibration outputs which are cabled to another pair of rotary switches on the cabinet front panel. The selected output is then connected to the dc null meter for calibration.

(3) Calibration Voltmeter Assembly

This assembly consists of two Hewlett Packard voltmeters: an HP 3406A sampling voltmeter to measure the RF and IF signal levels in the receiver, and an HP 419A null meter to measure the dc outputs from the detector and integrator circuits. Both units accept signals from the voltmeter switch assembly previously described.

The HP 3406A sampling voltmeter is capable of measuring RF signals from 1 kHz to 1 GHz. The voltage range (1 mv to 1 full scale) is spanned in seven pushbutton-selected steps of 10 dB each. An auxiliary dc output proportional to the meter deflection is provided and will be a useful feature in the event that there is a requirement at some future date to record calibration data.

The HP 419A dc null meter is capable of measuring voltages from ±3 mv to ±1000 v end scale in 18 ranges, each selected by means of a rotary switch. It has a minimum resolution capability of 0.1 μv; daily drift is less than 0.5 μv after warmup.

d. Frequency Synthesizer Unit

The first LO unit derives its signal from an HP 5100A synthesizer and an HP 5110A driver system. This synthesizer satisfies the following requirements:

1. It covers the required first local oscillator frequency range of 15 to 47 MHz.
2. Incremental frequency steps may be selected as small as 0.01 Hz, although this receiver requires that frequencies be selected in no less than 1-kHz increments.
3. Frequency selection may be accomplished either locally or remotely with a switching time of less than 1 ms.
4. Nonharmonically related spurious signals are down 90 dB or more from the selected output signal.

Operation of the frequency synthesizer is quite simple: the output frequency may be selected locally by 10 columns of pushbuttons. Any frequency that can be selected by the pushbuttons can also be programmed remotely. Three 50-pin connectors on the rear of the synthesizer provide connections for remote frequency selection. A local/remote switch determines control precedence when both methods are employed. A lock/operate switch prevents accidental operation of the pushbuttons. A self-checking capability is built into the synthesizer and the driver.

e. First Local Oscillator Unit

The first LO unit accepts the output signal from the frequency synthesizer unit, amplifies it, and supplies this signal at a maximum power level of 1 W to the first mixer of each of the receiver's two channels. Remotely switchable stopband filters are included in the signal path to reduce the level of noise in the synthesizer output at each of the three first IF's in order to prevent masking of low-level signals (Figure 29).

(1) Stopband Filter Design

The stopband filters were required to have the characteristics listed in Table IX.

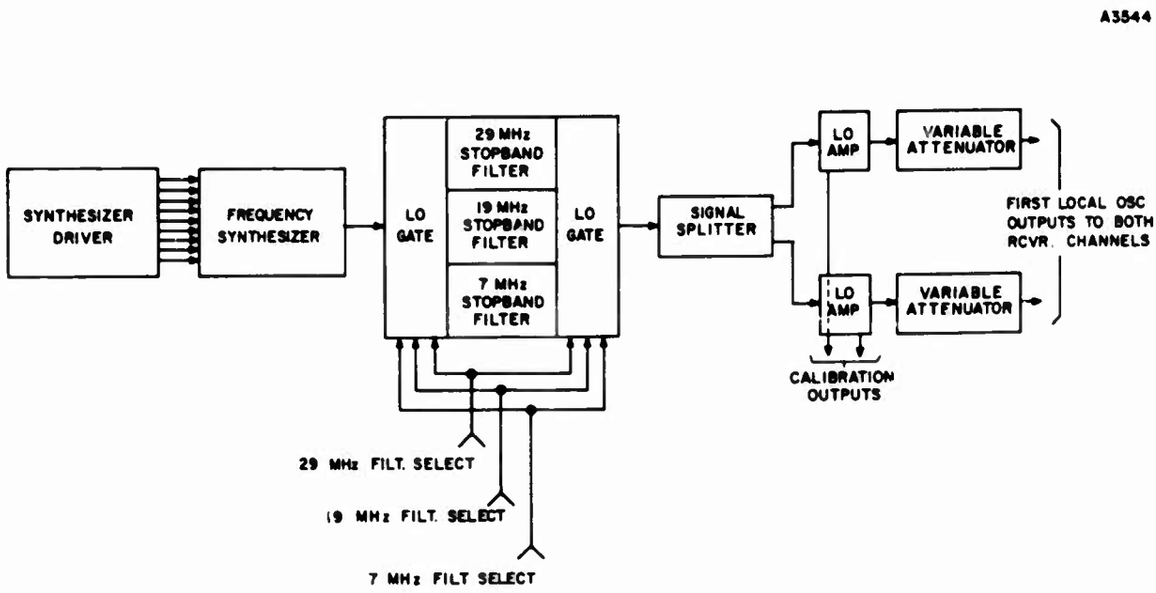


Figure 29. First Local Oscillator

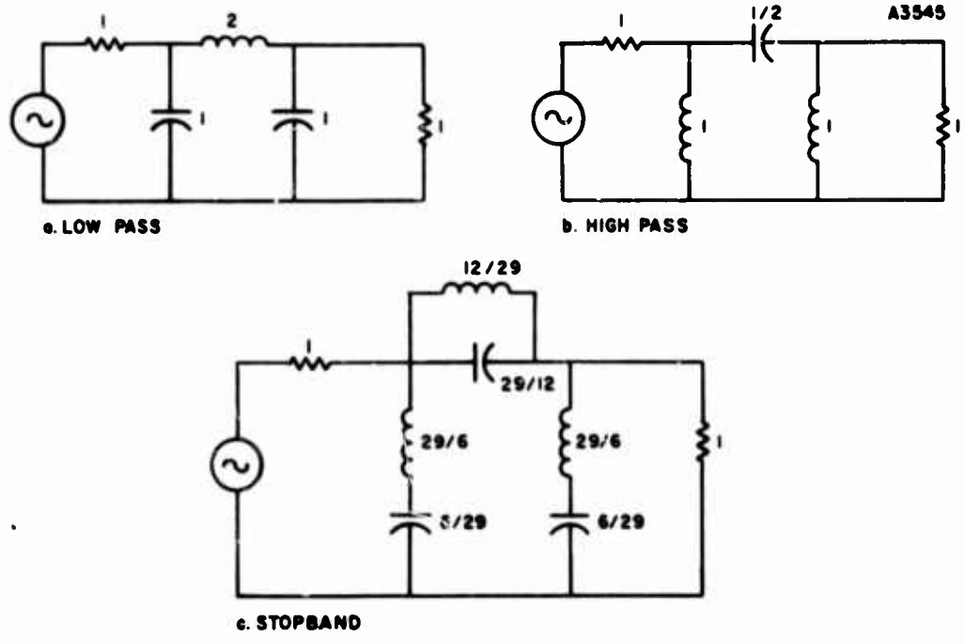


Figure 30. Stopband Filter Prototype Circuits

TABLE IX

STOPBAND FILTER CHARACTERISTICS

Center Frequency (MHz)	Nearest Desired Signal (MHz)	Attenuation Required (dB)
29	33	40
19	24	40
7	15	40
3	10	40

A third-order filter structure was deemed sufficient for this design. This was arrived at by trading off rejection band skirt slopes against filter bandwidth and realizable element values.

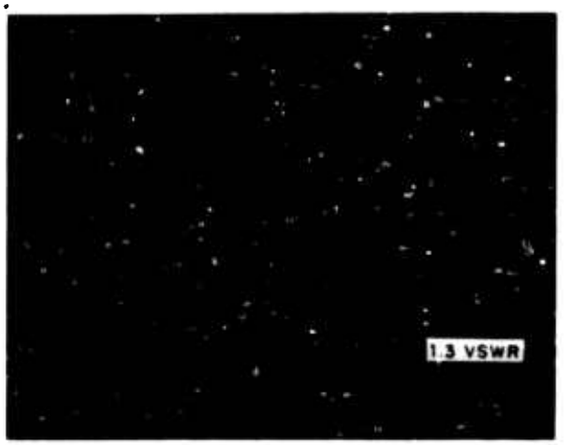
The design procedure used involved use of a low-pass prototype, mapping into a high-pass configuration, and then finally mapping into the stopband filter structure. Following this, the design was denormalized to achieve the desired impedance and frequency parameters.

The third-order Butterworth low-pass prototype circuit is shown in Figure 30a. The high-pass transformation yields the circuit shown in Figure 30b. Choosing a 6-MHz, 3-dB bandwidth for the stopband response means that the filter Q at 29 MHz will have a maximum value of 29/6, or approximately 5.0. Multiplying all elements in the high-pass prototype by this filter Q and then resonating the elements at $\omega = 1$ yields the circuit prototype shown in Figure 30c.

Denormalizing the element values of the stopband prototype will yield a filter with the desired center frequency and impedance level. By maintaining a constant filter Q, the same prototype may be used to design filters at the four required frequencies: 29, 19, 7, and 3 MHz.

The final measurements indicated notch depths of 39 dB for the 29-MHz filter, 40 dB for the 19-MHz filter, and 43 dB for the 7-MHz design. The 3-MHz design gave a 40-dB notch depth. The response and VSWR performance of the filters are shown in Figure 31.

a. 29 MHz



b. 19 MHz

c. 7 MHz

d. 3 MHz

Figure 31. Filter Characteristics

(2) Local Oscillator Power Amplifier

The output levels of both the first and second LO units are amplified to the level required by the respective mixers by a solid state 1-W power amplifier. This unit is manufactured by L.E.L., Inc., and consists of a single printed circuit board.

The performance specifications for this device are given in Table X.

TABLE X

POWER AMPLIFIER SPECIFICATIONS

Frequency range	10 to 47 MHz minimum
Gain at 1 W power output with 50-ohm source and load impedance	30 dB minimum
Power output variation across frequency range	±0.5 dB maximum
Gain compression at 1.5 W output power with 50-ohm source and load impedance	1 dB maximum
Input and output impedance	50 ohm nominal
Input VSWR	1.5 maximum
Output VSWR	2.0 maximum
Device complement	All solid state

Design details -- lacking at this time due to difficulties which the manufacturer is encountering in the design of this amplifier -- will be discussed in greater detail in a future report.

f. Second Local Oscillator Unit

The second LO unit shown in Figure 32 is similar in makeup to the first LO unit except that three separate fixed-frequency signal paths are provided, one for each of the three required second LO frequencies. Again, two 1-W outputs are provided at each frequency, one for each of the six second mixers employed in the receiver's dual channels.

The second LO frequency source is a high stability solid state unit manufactured by Frequency Electronics, Inc. The unit is a lightweight, compact plug-in module using a conventional octal base. Frequency stability on the order of ± 2 parts per 10^8 per 24 hours is realized by means of an automatic gain control loop around the oscillator transistor, insuring a constant drive level to compensate for component drift.

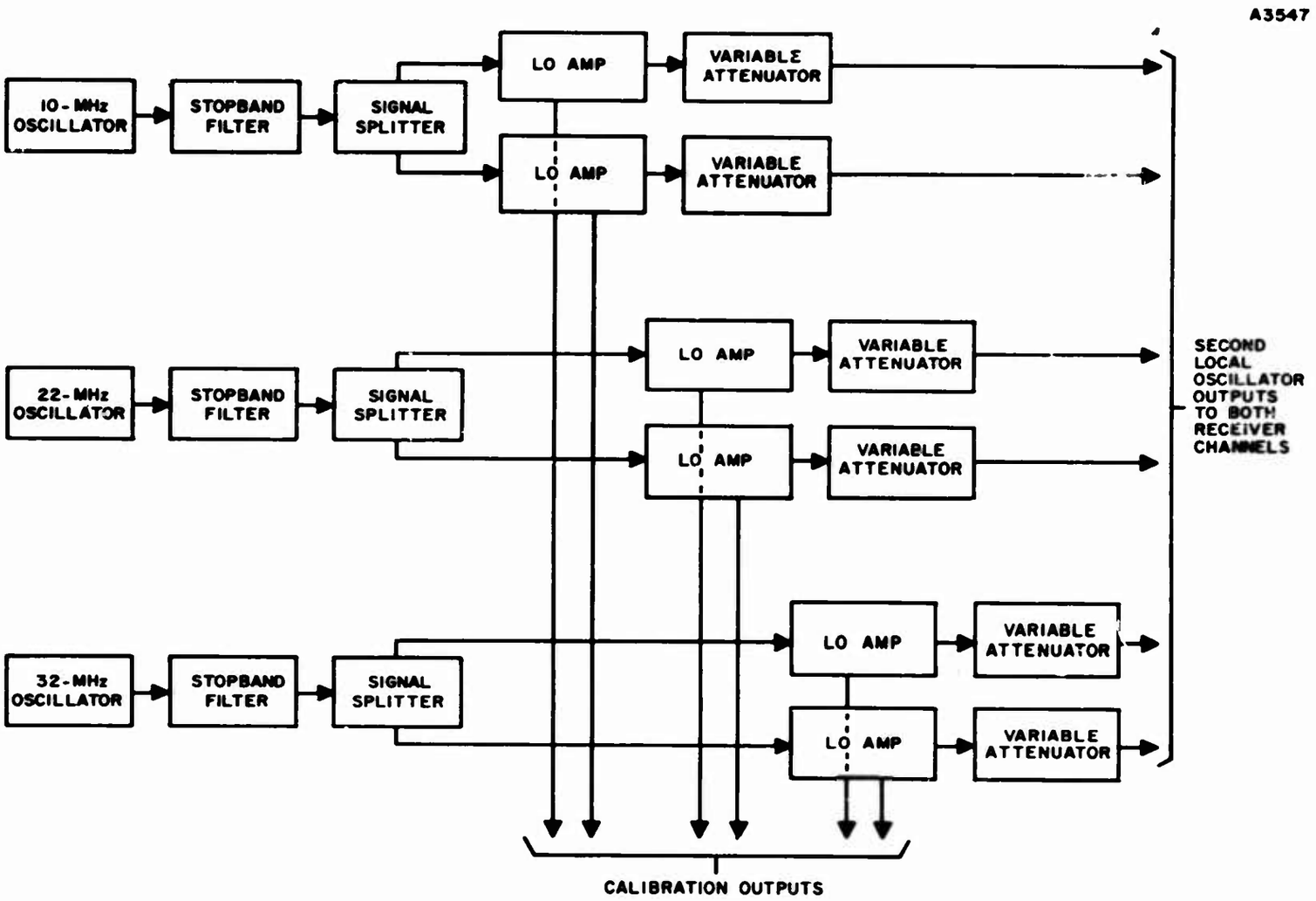


Figure 32. Second Local Oscillator

Two stages of buffering minimize the effect of load variation on frequency; in addition, a proportionally-controlled oven maintains the crystal temperature within 0.001°C/°C of ambient temperature variation. While the same power supply is used for both oven and oscillator circuits, oven noise or other interference is attenuated to a level at least 80 dB below the oscillator output level.

3. GENERAL DISCUSSION OF RECEIVER DIGITAL CONTROL UNIT

a. Functions

The functions of the digital control logic are:

1. To control the Hewlett Packard 5100 frequency synthesizer,
2. To select the proper RF filter in each channel,
3. To select the proper RF gate and IF gate in each channel, and
4. To provide the digital processor with information about the frequency that is being monitored.

b. Inputs

Primary control of the digital control unit is from the noise/interference receiver control panel located in cabinet 51. Additional timing and control signals come from the digital processor. In the manual mode of operation, frequency selection is controlled from a set of thumbwheel switches at the noise/interference receiver digital control cabinet.

(1) Control Panel

The controls on the noise/interference (N/I) receiver control panel are listed in Table XI (see Figure 33).

TABLE XI

NOISE/INTERFERENCE RECEIVER CONTROLS

Experiment Control Switches[1]	N/I automatic mode Manual mode CCIR mode Calibrate mode Integrator zero
Data Recorder Control Switches	Record start Record stop

1. These switches control the mode of operation for the N/I receiver.

TABLE XI (continued)

NOISE/INTERFERENCE RECEIVER CONTROLS

Antenna Select Switches (Rotary)	Receiver channel 1 Horizontal array Vertical array Multiplex Calibrate CCIR 50-ohm load Receiver channel 2 Horizontal array Vertical array Multiplex Calibrate CCIR 50-ohm load
Site Selection Switches (Rotary)	Receiver channel 1 East site North site South site Receiver channel 2 East site North site South site
MUF Selection Switches (Thumbwheel)	10-MHz digit selection (0-4) Unit-MHz digit selection (0-9)
MUF Fraction Selection Switches	1.0 MUF 0.9 MUF 0.8 MUF 0.7 MUF 0.5 MUF
Integration Time Selection Switches	3.0 second 0.3 second

TABLE XI (concluded)

NOISE/INTERFERENCE RECEIVER CONTROLS

CCIR Frequency Offset Switches (Thumbwheel)[2]	5 MHz offset 10 MHz offset 20 MHz offset
Receiver Channel Amplitude Error Indicator[3]	Channel 1 error Channel 2 error
Receiver Channel Amplitude Error Reset[4]	Channel 1 error reset Channel 2 error reset
Antenna Selection Error	This indicator will be lit when the operator tries to multiplex the horizontal array and vertical array on both receiver channels. It is also lit when the operator tries to have both receiver channels look at the CCIR antenna.

(2) Digital Processor

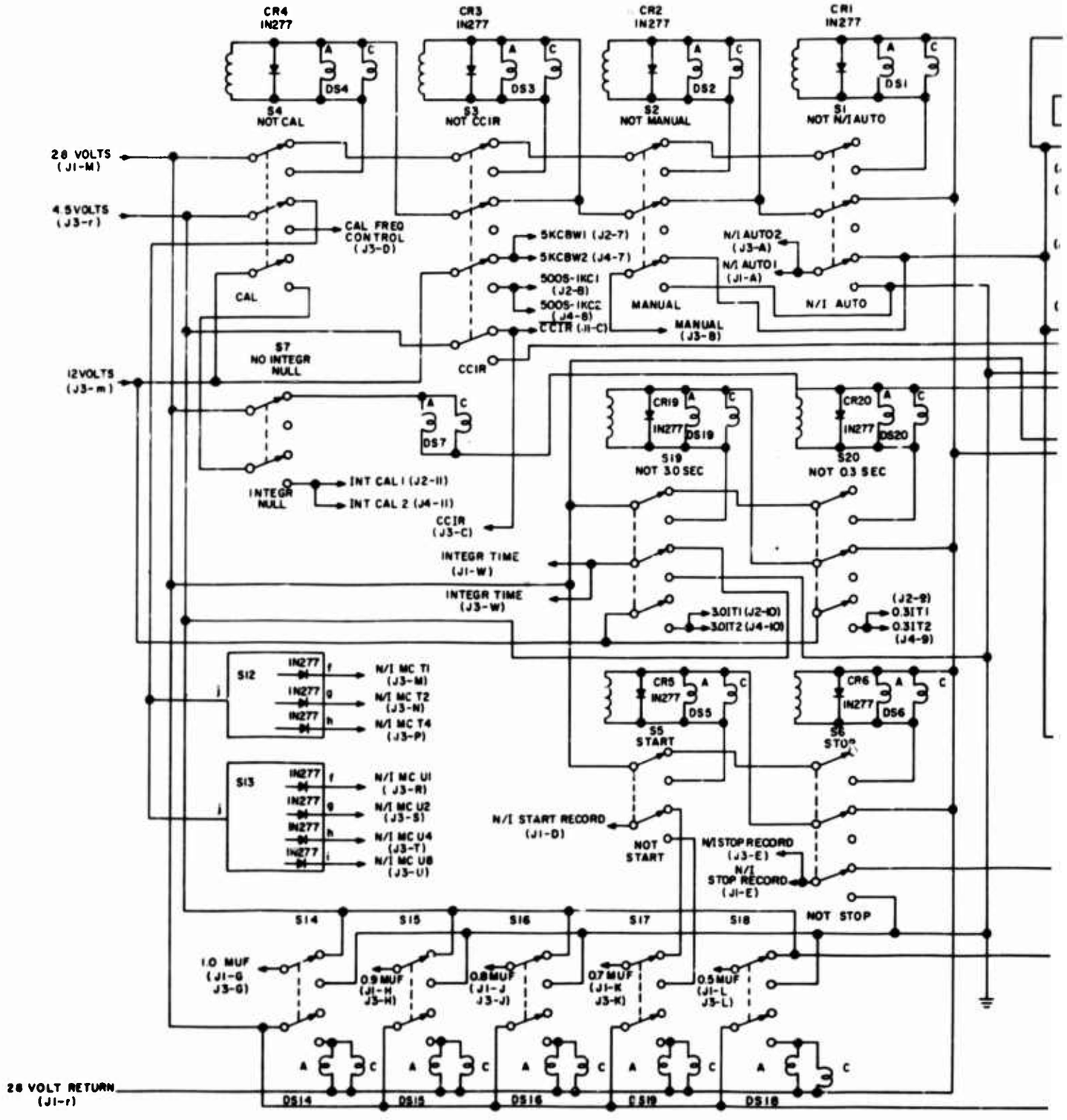
The following signals enter the N/I receiver digital control unit from the digital processor:

1. Fast timing signal -- this is a 100-kHz clock pulse signal that is used as the clock frequency in the N/I receiver digital control unit.

2. A/D timing signal -- this signal marks the end of an A/D converter timing cycle.

3. End N/I sample -- this signifies that the digital processor has completed sampling the output of both receiver channels.

2. These switches allow the CCIR frequencies to be offset by 0 to 9 kHz in 1-kHz steps.
3. These lights show when the signals in the receiver channels are too large; the lights are controlled from the digital processor.
4. These switches reset the receiver channel amplitude error indicators.


CR4 IN277
CR3 IN277
CR2 IN277
CR1 IN277
DS4
DS3
DS2
DS1
S4 NOT CAL
S3 NOT CCIR
S2 NOT MANUAL
S1 NOT N/I AUTO
28 VOLTS (J1-M)
4.5 VOLTS (J3-r)
CAL FREQ CONTROL (J3-D)
5KCBW1 (J2-7)
5KCBW2 (J4-7)
5005-IKC1 (J2-8)
5005-IKC2 (J4-8)
CCIR (J1-C)
N/I AUTO2 (J3-A)
N/I AUTO1 (J1-A)
MANUAL
N/I AUTO
MANUAL (J3-B)
CAL
S7 NO INTEGR NULL
12VOLTS (J3-m)
CCIR
DS7
CR19 IN277 DS19
CR20 IN277 DS20
S19 NOT 3.0 SEC
S20 NOT 0.3 SEC
INTEGR NULL
INT CAL 1 (J2-11)
INT CAL 2 (J4-11)
CCIR (J3-C)
INTEGR TIME (J1-W)
INTEGR TIME (J3-W)
3.0IT1 (J2-10)
3.0IT2 (J4-10)
(J2-9) 0.3IT1
0.3IT2 (J4-9)
S12
S13
N/I MC T1 (J3-M)
N/I MC T2 (J3-N)
N/I MC T4 (J3-P)
N/I MC U1 (J3-R)
N/I MC U2 (J3-S)
N/I MC U4 (J3-T)
N/I MC U8 (J3-U)
CR5 IN277 DS5
CR6 IN277 DS6
S5 START
S6 STOP
N/I START RECORD (J1-D)
NOT START
N/I STOP RECORD (J3-E)
N/I STOP RECORD (J1-E)
NOT STOP
S14
S15
S16
S17
S18
1.0 MUF (J1-G J3-G)
0.9 MUF (J1-H J3-H)
0.8 MUF (J1-J J3-J)
0.7 MUF (J1-K J3-K)
0.5 MUF (J1-L J3-L)
28 VOLT RETURN (J1-r)
DS14
DS15
DS16
DS17
DS18

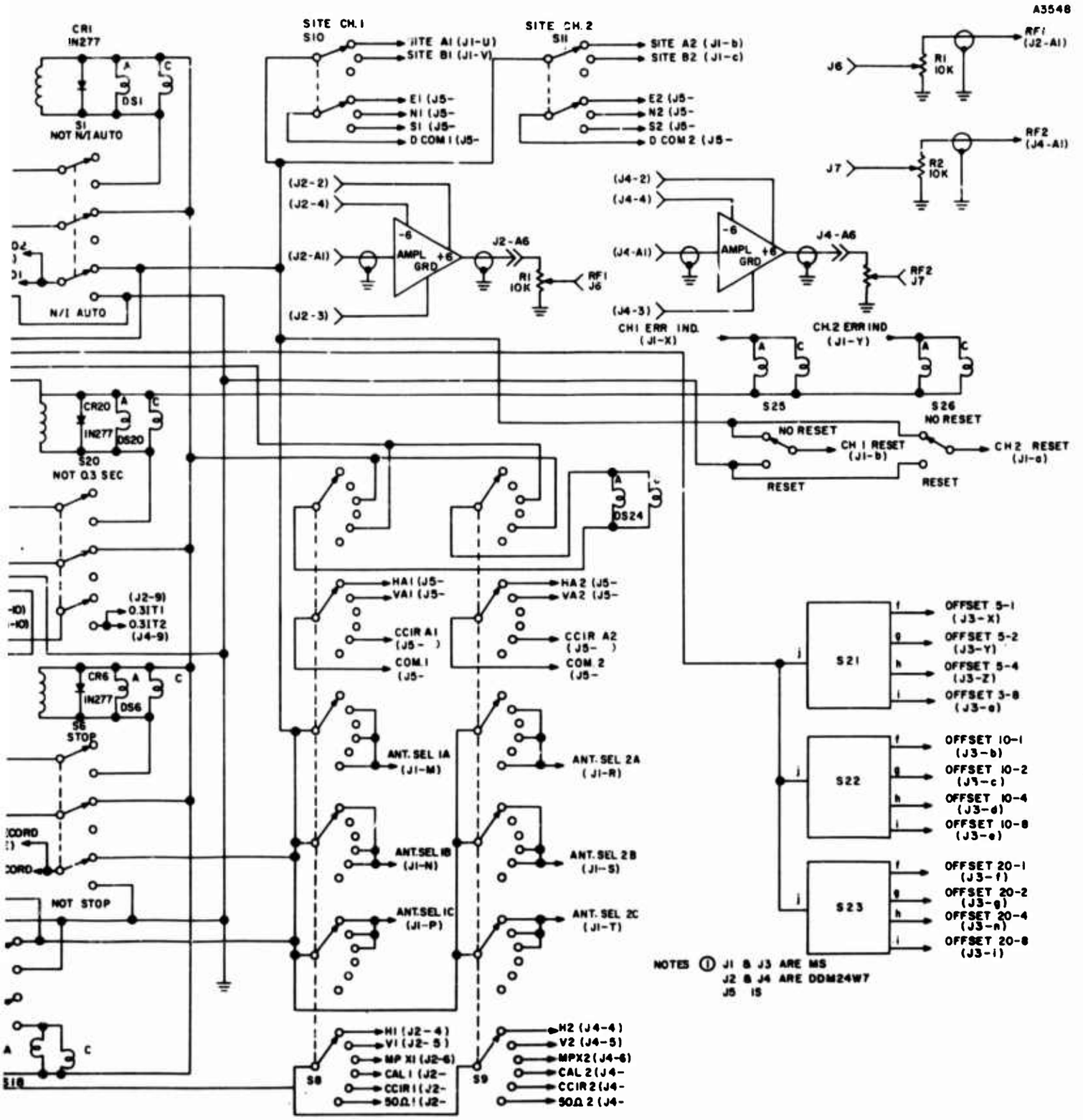


Figure 33. Control Panel

4. Integration timing -- this signal arrives at the selected (0.3-, 3.0-, 500-second) integration timing.

5. N/I multiplex -- this signal determines whether the receiver channel looks at the horizontal array or the vertical array in the multiplex mode.

c. Outputs

(1) RF Filter Selection

The N/I receiver digital control unit uses 36 lines to select one of 36 1-MHz RF filters in each receiver channel. Two additional signals are used to signify whether the selected RF filter lies in the lower half of the band (4 to 21 MHz) or in the upper half of the band (22 to 39 MHz).

(2) IF Filter Selection

The N/I receiver digital control unit selects one of three (7-, 19-, 29-MHz) IF processing chains to be used in each receiver channel. The selection is determined by the RF being analyzed.

(3) Hewlett Packard Synthesizer

The N/I receiver digital control unit selects the 10-MHz (0-4), unit-MHz, 100-kHz, 10-kHz, and unit-kHz digits of the synthesizer. In the automatic mode, the synthesizer is stepped in 4-kHz increments. In the manual mode the synthesizer can be set to the nearest kHz.

(4) Digital Processor

1. Record data -- this signal tells the digital processor to record data.

2. Binary MUF frequency -- the MUF, in binary code, as selected by the operator is recorded on the magnetic tape.

3. The MUF fraction that is being processed is recorded on magnetic tape.

4. The actual frequency, in binary code, that is being monitored is recorded on magnetic tape. [It is not absolutely necessary to record this. It was felt that a quick check on some of the logic in the control unit could be made by comparing the monitored frequency with items (2) and (3) above.]

5. CCIR frequency -- in the CCIR mode of operation, the CCIR frequency is recorded on magnetic tape.

TABLE XII

TRUTH TABLE, BCD TO BINARY

Frequency (MHz)	BCD CODE							BINARY CODE					
	T4	T2	T1	U8	U4	U2	U1	B6	B5	B4	B3	B2	B1
40	1	0	0	0	0	0	0	1	0	1	0	0	0
39	0	1	1	1	0	0	1	1	0	0	1	1	1
38	0	1	1	1	0	0	0	1	0	0	1	1	0
37	0	1	1	0	1	1	1	1	0	0	1	0	1
36	0	1	1	0	1	1	0	1	0	0	1	0	0
35	0	1	1	0	1	0	1	1	0	0	0	1	1
34	0	1	1	0	1	0	0	1	0	0	0	1	0
33	0	1	1	0	0	1	1	1	0	0	0	0	1
32	0	1	1	0	0	1	0	1	0	0	0	0	0
31	0	1	1	0	0	0	1	0	1	1	1	1	1
30	0	1	1	0	0	0	0	0	1	1	1	1	0
29	0	1	0	1	0	0	1	0	1	1	1	0	1
28	0	1	0	1	0	0	0	0	1	1	1	0	0
27	0	1	0	0	1	1	1	0	1	1	0	1	1
26	0	1	0	0	1	1	0	0	1	1	0	1	0
25	0	1	0	0	1	0	1	0	1	1	0	0	1
24	0	1	0	0	1	0	0	0	1	1	0	0	0
23	0	1	0	0	0	1	1	0	1	0	1	1	1
22	0	1	0	0	0	1	0	0	1	0	1	1	0
21	0	1	0	0	0	0	1	0	1	0	1	0	1
20	0	1	0	0	0	0	0	0	1	0	1	0	0
19	0	0	1	1	0	0	1	0	1	0	0	1	1
18	0	0	1	1	0	0	0	0	1	0	0	1	0
17	0	0	1	0	1	1	1	0	1	0	0	0	1
16	0	0	1	0	1	1	0	0	1	0	0	0	0
15	0	0	1	0	1	0	1	0	0	1	1	1	1
14	0	0	1	0	1	0	0	0	0	1	1	1	0
13	0	0	1	0	0	1	1	0	0	1	1	0	1
12	0	0	1	0	0	1	0	0	0	1	1	0	0
11	0	0	1	0	0	0	1	0	0	1	0	1	1
10	0	0	1	0	0	0	0	0	0	1	0	1	0
9	0	0	0	1	0	0	1	0	0	1	0	0	1
8	0	0	0	1	0	0	0	0	0	1	0	0	0
7	0	0	0	0	1	1	1	0	0	0	1	1	1
6	0	0	0	0	1	1	0	0	0	0	1	1	0
5	0	0	0	0	1	0	1	0	0	0	1	0	1
4	0	0	0	0	1	0	0	0	0	0	1	0	0

4. DETAILED DESIGN

a. BCD to Binary Frequency Conversion

Figure 34 shows the boards that process the tens digit and the units digit of the frequency to be processed by the receiver channels.

In the manual mode the input comes from frequency selection switches which are on a panel at the top of the cabinet which contains the N/I receiver digital control equipment. In the automatic mode the frequency is selected from the N/I control panel. The information is in binary-coded-decimal (BCD) form.

The BCD frequency to binary frequency board converts the BCD numbers to binary numbers. Table XII snows the truth table for this conversion.

The board implements the following equations:

$$B1 = U1$$

$$B2 = \overline{T1} \cdot U2 + T1 \cdot \overline{U2}$$

$$B3 = \overline{T1} \cdot \overline{T2} \cdot U4 + \overline{T1} \cdot T2 \cdot \overline{U4} + T1 \cdot \overline{T2} \cdot \overline{U2} \cdot U4 + T1 \cdot \overline{T2} \cdot U2 \cdot \overline{U4} + T1 \cdot T2 \cdot U2 \cdot U4 + T1 \cdot T2 \cdot \overline{U2} \cdot \overline{U4}$$

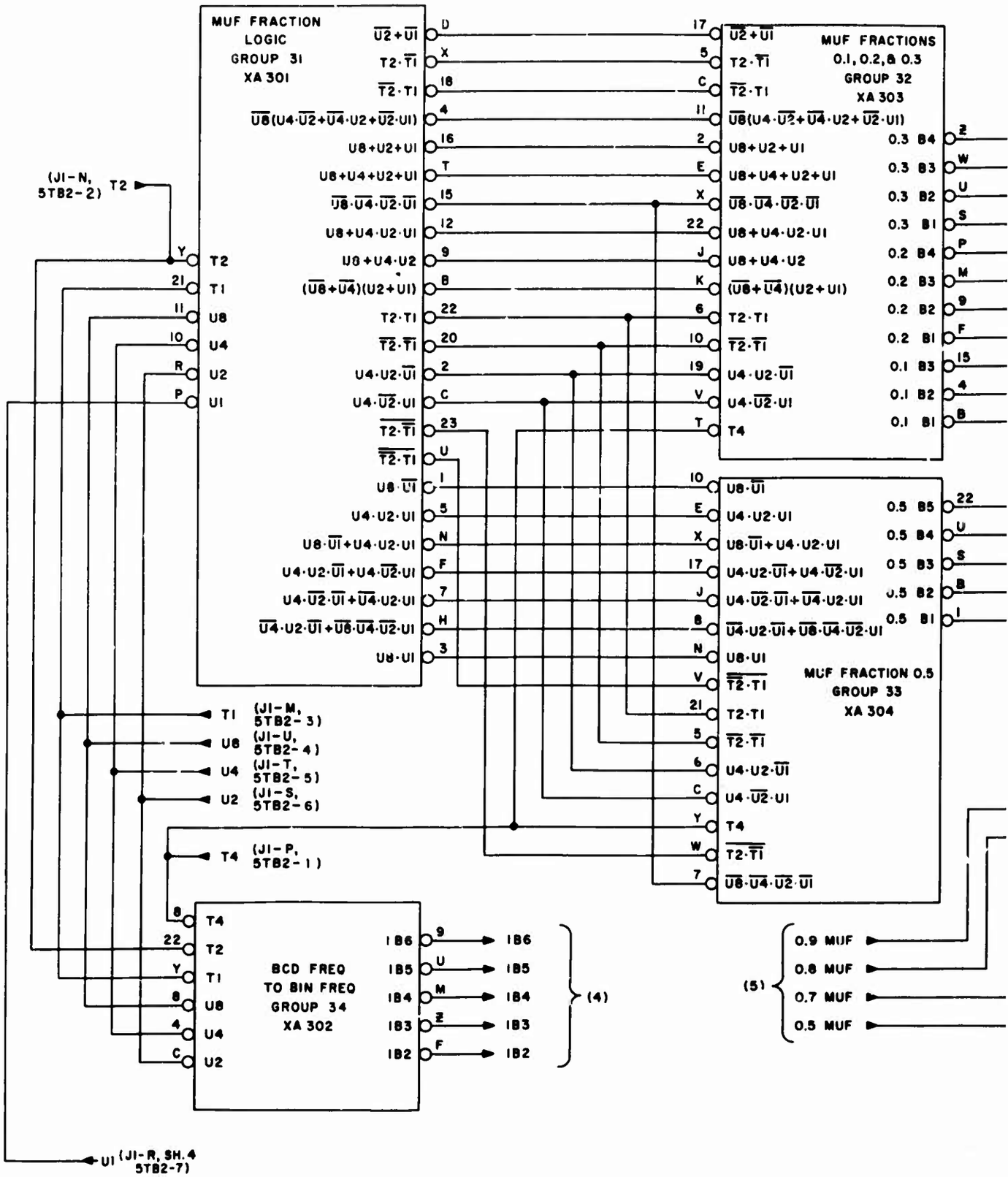
$$B4 = T4 + T1 \cdot T2 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{T1} \cdot T2 \cdot (U4 + U8) + T1 \cdot \overline{T2} \cdot \overline{U4} \cdot \overline{U8} + T1 \cdot \overline{T2} \cdot \overline{U2} \cdot \overline{U8} + \overline{T1} \cdot \overline{T2} \cdot U8$$

$$B5 = T2 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{T1} \cdot T2 + T1 \cdot \overline{T2} \cdot U8 + T1 \cdot \overline{T2} \cdot U2 \cdot U4$$

$$B6 = T4 + T1 \cdot T2 \cdot (U2 + U4 + U8)$$

The logic diagram for the BCD frequency to binary frequency conversion board is shown in Figure 35.

The output of the BCD frequency to binary frequency converter goes to a set of gates shown in Figure 36. If the receiver is not in the CCIR mode of operation, the output of the gate will be the binary number output of the BCD frequency to binary frequency converter. In the CCIR mode of operation, the gate output will be a binary 5, 10, or 20, depending on the CCIR frequency that is to be monitored. This gate provides one set of inputs to a six-bit binary adder shown in Figure 37.


MUF FRACTION LOGIC GROUP 31 XA 301
MUF FRACTIONS 0.1, 0.2, & 0.3 GROUP 32 XA 303
MUF FRACTION 0.5 GROUP 33 XA 304
BCD FREQ TO BIN FREQ GROUP 34 XA 302
(JI-N, 5TB2-2) T2
T1 (JI-M, 5TB2-3)
U8 (JI-U, 5TB2-4)
U4 (JI-T, 5TB2-5)
U2 (JI-S, 5TB2-6)
T4 (JI-P, 5TB2-1)
U1 (JI-R, SH. 4 5TB2-7)
(4)
(5)
0.9 MUF
0.8 MUF
0.7 MUF
0.5 MUF

1

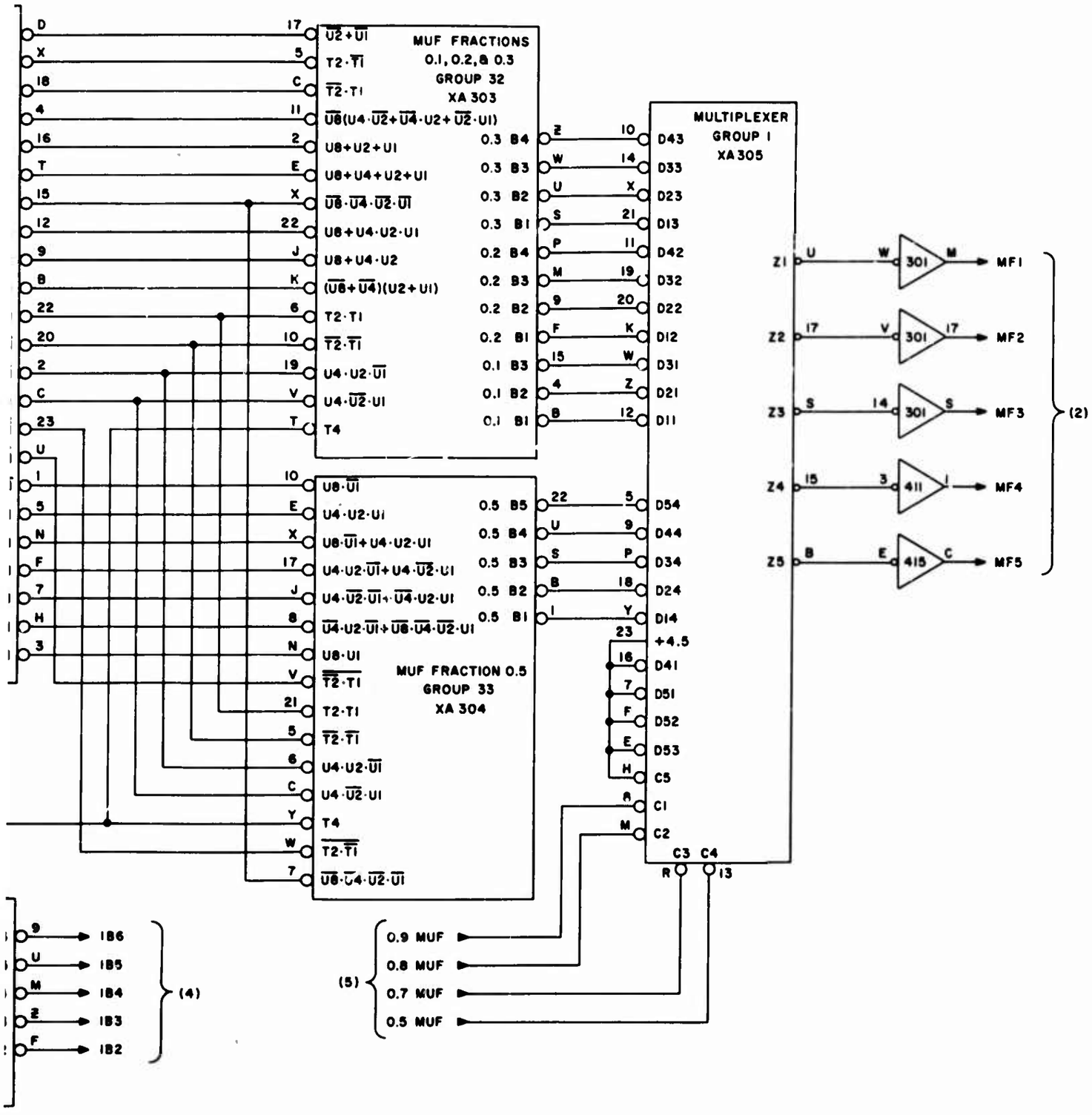
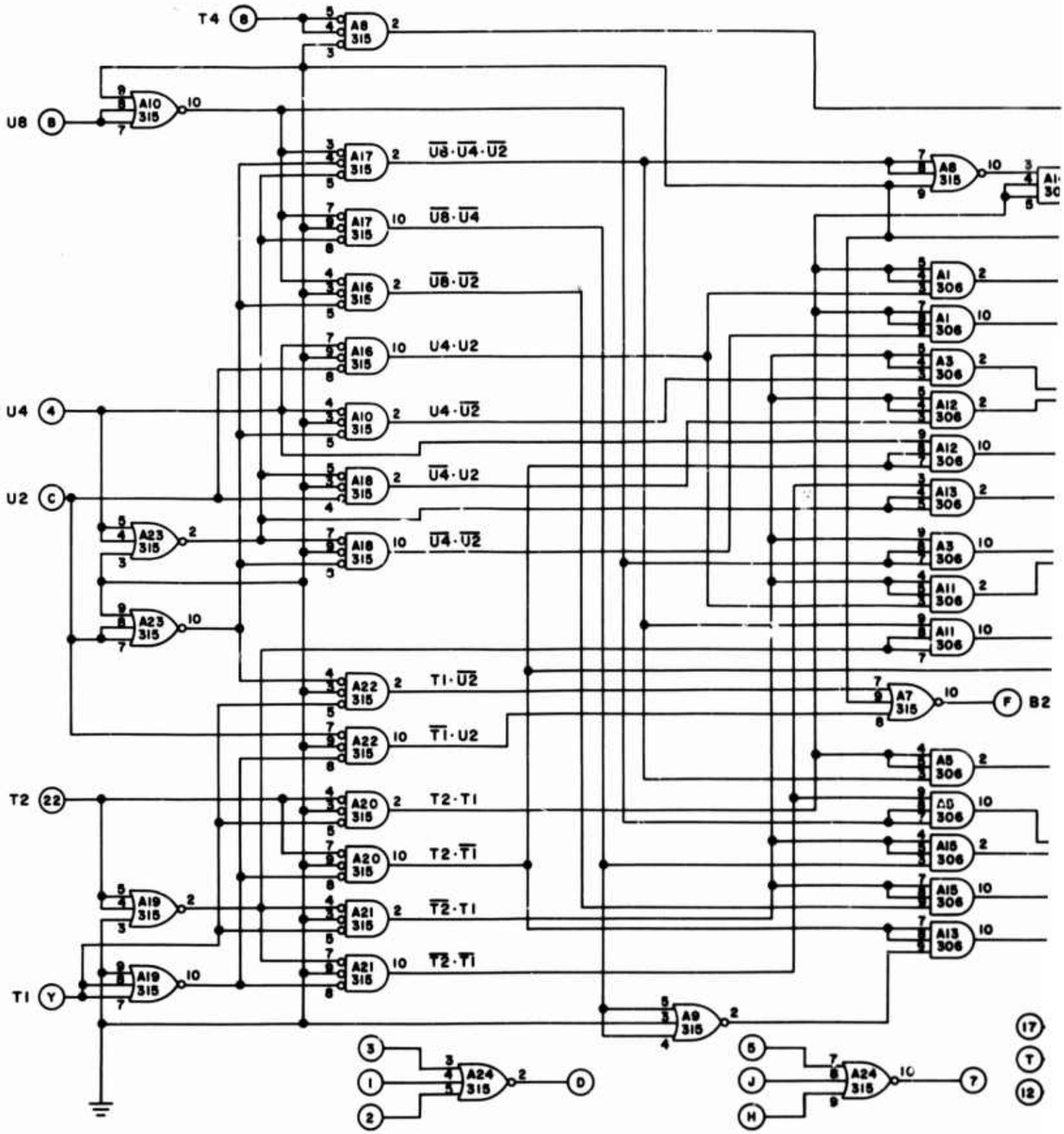


Figure 34. Tens Digit and Units Digital Processing


T4
U8
U4
U2
T2
T1
A8 315
A10 315
A17 315
A16 315
A10 315
A18 315
A23 315
A22 315
A20 315
A19 315
A21 315
A24 315
A9 315
A1 306
A3 306
A12 306
A13 306
A5 306
A11 306
A15 306
A7 315
U8·U4·U2
U8·U4
U8·U2
U4·U2
U4·U2
U4·U2
U4·U2
T1·U2
T1·U2
T2·T1
T2·T1
T2·T1
T2·T1
F
B2

Figure

1

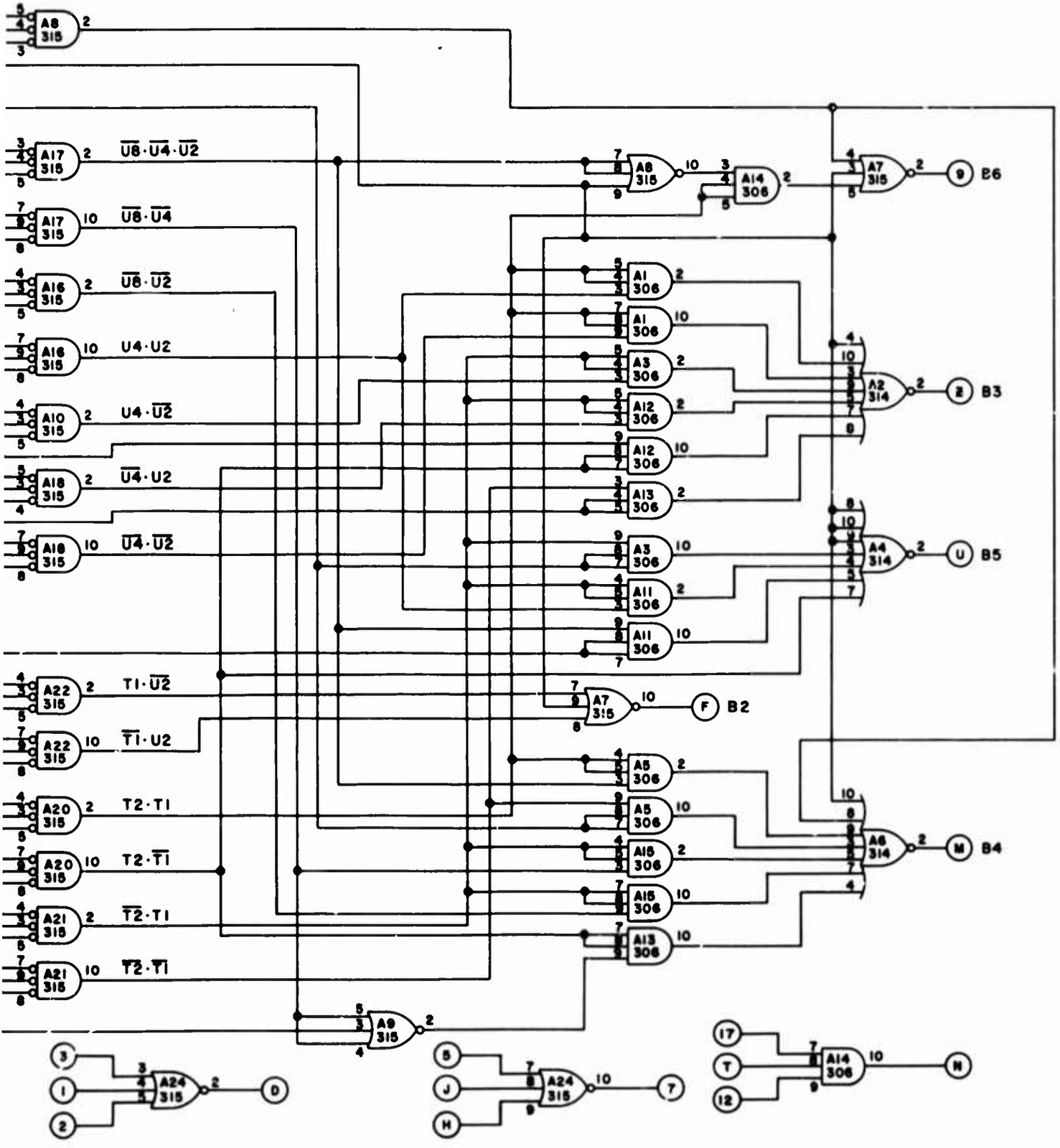
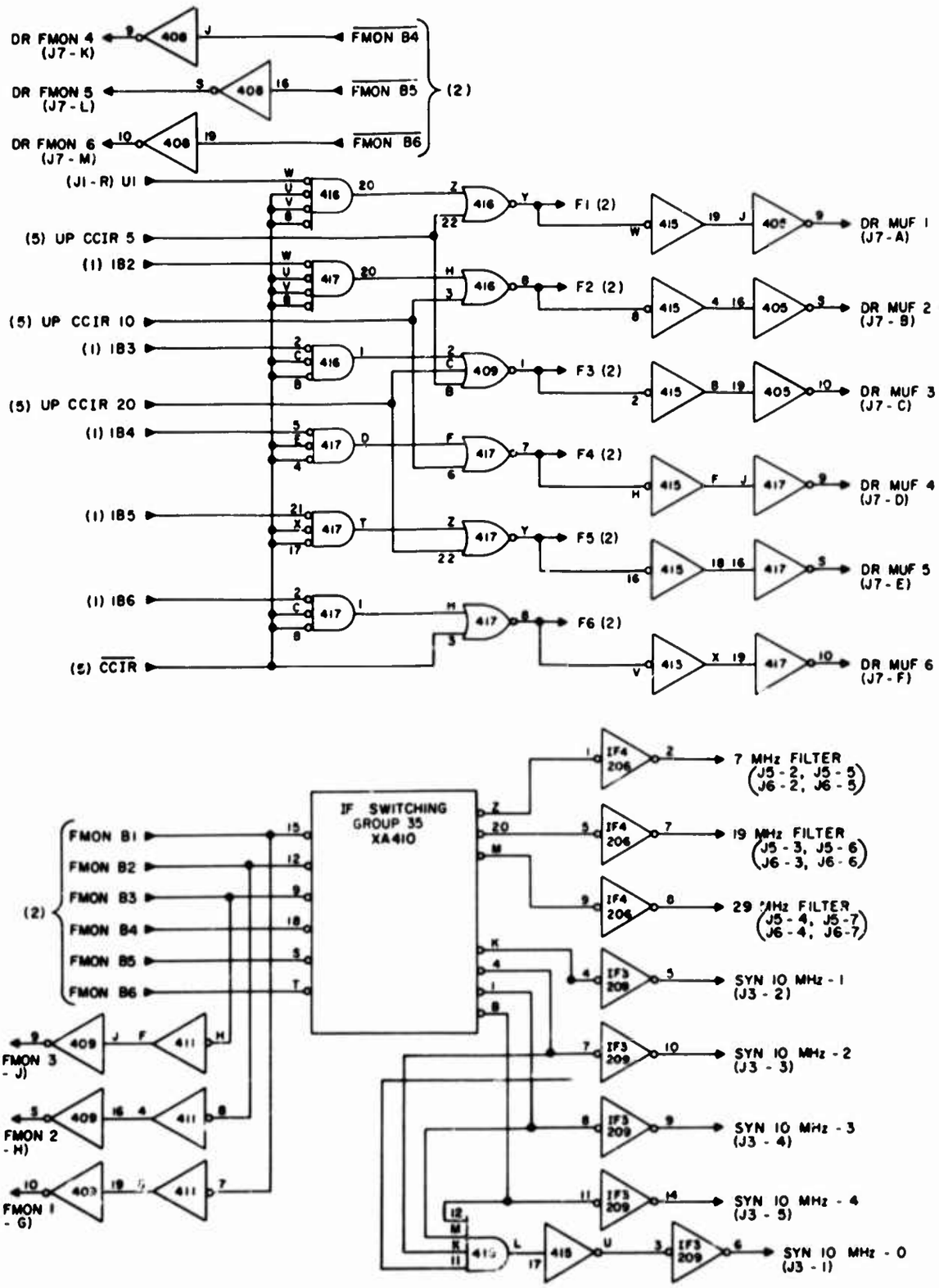


Figure 35. BCD to Binary Frequency Conversion

2


DR FMON 4 (J7 - K)
DR FMON 5 (J7 - L)
DR FMON 6 (J7 - M)
FMON B4
FMON B5
FMON B6
(2)
(J1 - R) U1
(5) UP CCIR 5
(1) IB2
(5) UP CCIR 10
(1) IB3
(5) UP CCIR 20
(1) IB4
(1) IB5
(1) IB6
(5) CCIR
F1 (2)
F2 (2)
F3 (2)
F4 (2)
F5 (2)
F6 (2)
DR MUF 1 (J7 - A)
DR MUF 2 (J7 - B)
DR MUF 3 (J7 - C)
DR MUF 4 (J7 - D)
DR MUF 5 (J7 - E)
DR MUF 6 (J7 - F)
11 M
21 M
33 M
22 M
34 M
13 M
23 M
35 M
4 M
14 M
24 M
36 M
5 M
15 M
25 M
37 M
6 M
8 M
16 M
18 M
26 M
28 M
38 M
7 M
9 M
17 M
19 M
27 M
29 M
39 M
30 M
31 M
10 M
12 M
20 M
32 M
FMON B1
FMON B2
FMON B3
FMON B4
FMON B5
FMON B6
DR FMON 3 (J7 - J)
DR FMON 2 (J7 - H)
DR FMON 1 (J7 - G)
IF SWITCHING GROUP 35 XA410
7 MHz FILTER (J5 - 2, J5 - 5) (J6 - 2, J6 - 5)
19 MHz FILTER (J5 - 3, J5 - 6) (J6 - 3, J6 - 6)
29 MHz FILTER (J5 - 4, J5 - 7) (J6 - 4, J6 - 7)
SYN 10 MHz - 1 (J3 - 2)
SYN 10 MHz - 2 (J3 - 3)
SYN 10 MHz - 3 (J3 - 4)
SYN 10 MHz - 4 (J3 - 5)
SYN 10 MHz - 0 (J3 - 1)

1

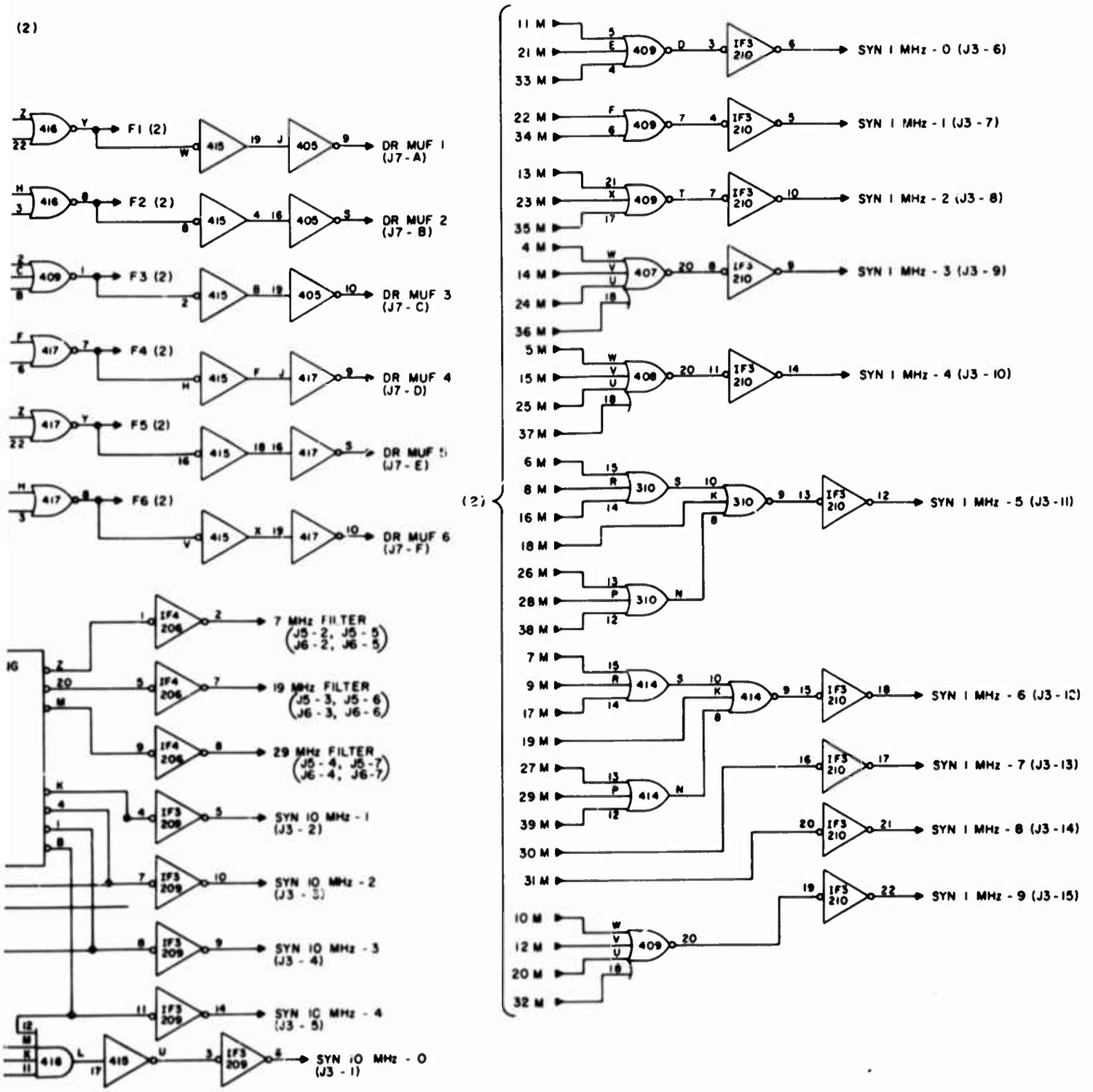


Figure 36. Switching Logic

2

4 MHz FILTER (J2-4; J4-4)
5 MHz FILTER (J2-5; J4-5)
6 MHz FILTER (J2-6; J4-6)
7 MHz FILTER (J2-7; J4-7)
8 MHz FILTER (J2-8; J4-8)
9 MHz FILTER (J2-9; J4-9)
10 MHz FILTER (J2-10; J4-10)
11 MHz FILTER (J2-11; J4-11)
12 MHz FILTER (J2-12; J4-12)
13 MHz FILTER (J2-13; J4-13)
14 MHz FILTER (J2-14; J4-14)
15 MHz FILTER (J2-15; J4-15)
16 MHz FILTER (J2-16; J4-16)
17 MHz FILTER (J2-17; J4-17)
18 MHz FILTER (J2-18; J4-18)
19 MHz FILTER (J2-19; J4-19)
20 MHz FILTER (J2-20; J4-20)
21 MHz FILTER (J2-21; J4-21)
22 MHz FILTER (J2-22; J4-22)
23 MHz FILTER (J2-23; J4-23)
24 MHz FILTER (J2-24; J4-24)
25 MHz FILTER (J2-25; J4-25)
26 MHz FILTER (J2-26; J4-26)
27 MHz FILTER (J2-27; J4-27)
28 MHz FILTER (J2-28; J4-28)
29 MHz FILTER (J2-29; J4-29)
30 MHz FILTER (J2-30; J4-30)
DECODE GROUP 6 XA308
DECODE GROUP 6 XA309
FMON B3 (4)
FMON B2 (4)
(4) FMON B6
(4) FMON B5
(4) FMON B4
FMON B4
(4) FMON B1
(4) F5
(4)F1
(1) MF1
(4) F2
MF2 (1)
(4)F3
MF3 (1)
(4)F4
MF4 (1)
MF5 (1)
ADDER GROUP 2 XA306

1

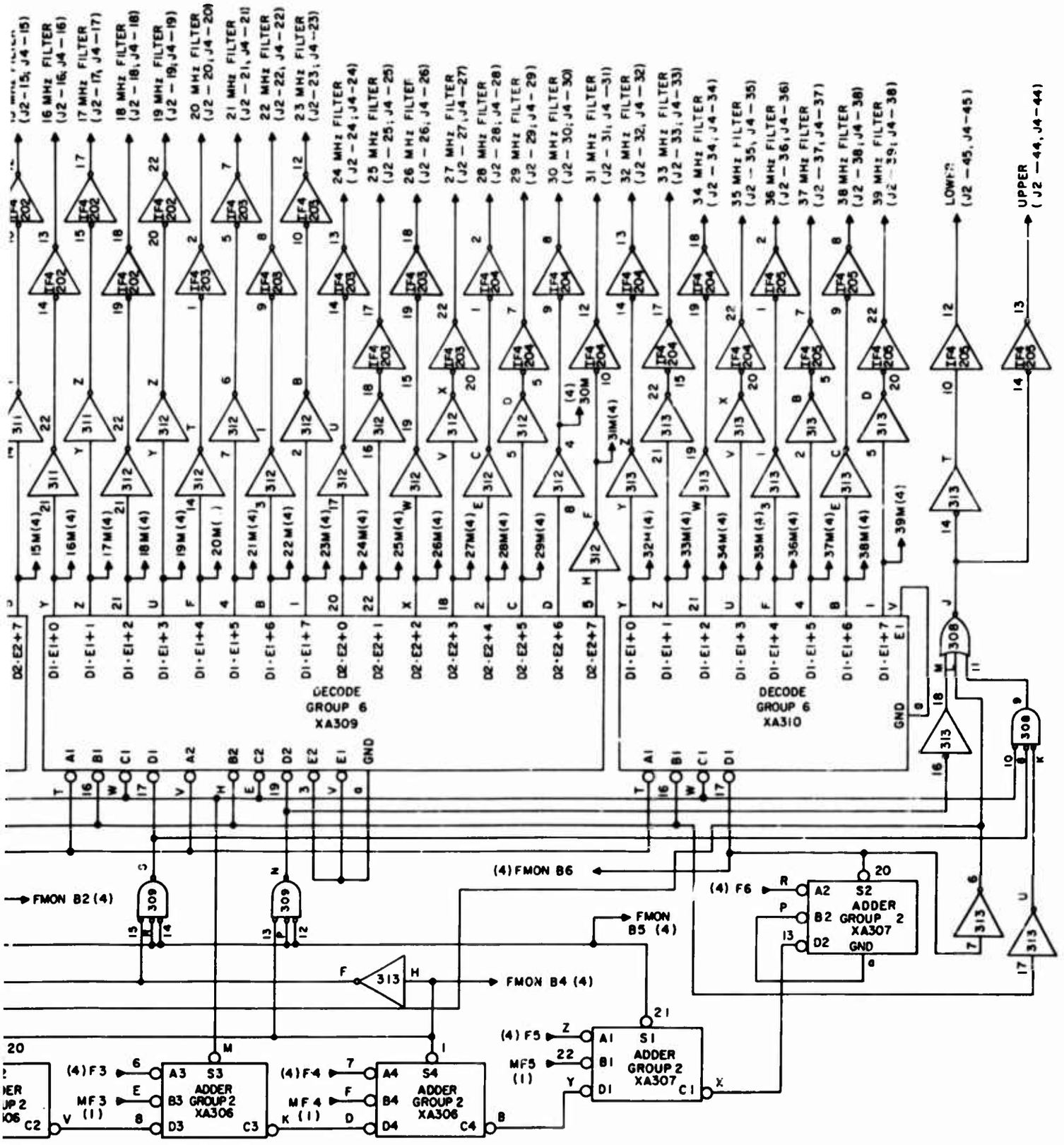


Figure 37. Decoding Logic

b. BCD To Binary Fraction Frequency Conversion

The BCD frequency is also decoded to provide 0.1, 0.2, 0.3, and 0.5 fractions of itself. The fractions are subtracted from the frequency to obtain the actual frequency (i.e., 0.9 MUF, 0.8 MUF, 0.7 MUF, 0.5 MUF) which controls the receiver channels. If no fraction is selected, the binary frequency (1.0 MUF) will control the receiver channels.

The fraction decoding is such to always round downwards. Table XIII shows the frequencies that will control the receiver for a particular MUF.

Three boards perform this decoding. The first board, MUF fraction logic, decodes a group of terms which are used to generate the binary fractions. The MUF fractions 0.1, 0.2, and 0.3 board actually generates the binary equivalent for 0.1 x MUF, 0.2 x MUF, and 0.3 x MUF.

The MUF function 0.5 board generates 0.5 x MUF.

The MUF fraction logic board generates the following functions:

Pin X $\overline{T1} \cdot T2$

Pin 18 $T1 \cdot \overline{T2}$

Pin 22 $T1 \cdot T2$

Pin 20 $\overline{T1 \cdot T2}$

Pin 23 $\overline{\overline{T1} \cdot T2}$

Pin U $\overline{T1 \cdot \overline{T2}}$

Pin D $\overline{U1} + \overline{U2}$

Pin 16 $U1 + U2 + U8$

Pin T $U1 + U2 + U4 + U8$

Pin 15 $\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}$

Pin 12 $U1 \cdot U2 \cdot U4 + U8$

Pin 9 $U2 \cdot U4 + U8$

Pin 2 $\overline{U1} \cdot U2 \cdot U4$

Pin C $U1 \cdot \overline{U2} \cdot U4$

Pin 1 $\overline{U1} \cdot U8$

Pin 5 $U1 \cdot U2 \cdot U4$

Pin 3 $U1 \cdot U8$

Pin 4 $(U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\,\overline{U8}$

Pin B $(U1 + U2)\,(\overline{U4} \cdot \overline{U8})$

TABLE XIII

TRUTH TABLE, MUF FRACTIONS

MUF	0.9 MUF	0.8 MUF	0.7 MUF	0.5 MUF
40	36	32	28	20
39	35	31	27	19
38	34	30	26	19
37	33	29	25	18
36	32	28	25	18
35	31	28	24	17
34	30	27	23	17
33	29	26	23	16
32	28	25	22	16
31	27	24	21	15
30	27	24	21	15
29	26	23	20	14
28	25	22	19	14
27	24	21	18	13
26	23	20	18	13
25	22	20	17	12
24	21	19	16	12
23	20	18	16	11
22	19	17	15	11
21	18	16	14	10
20	18	16	14	10
19	17	15	13	9
18	16	14	12	9
17	15	13	11	8
16	14	12	11	8
15	13	12	10	7
14	12	11	9	7
13	11	10	9	6
12	10	9	8	6
11	9	8	7	5
10	9	8	7	5
9	8	7	6	4
8	7	6	5	4
7	6	5	4	4
6	5	4	4	4
5	4	4	4	4
4	4	4	4	4

Pin N $U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8$

Pin F $U1 \cdot \overline{U2} \cdot U4 + \overline{U1} \cdot U2 \cdot U4$

Pin 7 $U1 \cdot U2 \cdot \overline{U4} + \overline{U1} \cdot \overline{U2} \cdot U4$

Pin H $U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}$

The detailed logic diagram for the MUF fraction logic board is shown in Figure 38.

The approach for generating the MUF fractions is to decode one line for each value that the fraction can have and then OR the proper lines to generate the binary value of the MUF fraction.

For example, 0.1 MUF can take on five possible values: 4, 3, 2, 1, and 0. The equations that show when 0.1 MUF should have these values are given below:

$$4 = T4 + T1 \cdot T2 \,(U1 + U2 + U4 + U8)$$

$$3 = T1 \cdot T2 \cdot (U1 + U2 + U4 + U8) + T1 \cdot T2 \,(U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\,\overline{U8}$$

$$2 = T1 \cdot \overline{T2} \cdot (U1 + U2 + U4 + U8) + \overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8})$$

$$1 = \overline{T1} \cdot \overline{T2} \cdot (U1 + U2 + U8) + T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8})$$

Bit 3 of 0.1 x MUF is then the 4 output.

Bit 2 of 0.1 x MUF is output 2 or output 3.

Bit 1 of 0.1 x MUF is output 1 or output 3.

If 0.1 MUF is zero the 1, 2, 3, and 4 outputs will be disabled causing bit 1, bit 2, and bit 3 outputs to be disabled which is equivalent to binary zero. Similarly, we can write the following equations.

Bit 4 of 0.2 MUF is equal to:

$$T4 + T1 \cdot T2 \,(U2 \cdot U4 + U8)$$

Bit 3 of 0.2 MUF is equal to:

$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\,\overline{U8} + T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + \overline{T1} \cdot T2 \cdot (U2 \cdot U4 + U8) + \overline{T1} \cdot T2 \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\,\overline{U8} + \overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + T1 \cdot \overline{T2}\,(U2 \cdot U4 + U8)$$

Bit 2 of 0.2 MUF is equal to:

$$\overline{T1} \cdot T2 \cdot (U2 \cdot U4 + U8) + T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\ \overline{U8} +$$
$$T1 \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\ \overline{U8} +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + \overline{T1} \cdot \overline{T2} \cdot (U2 \cdot U4 + U8)$$

Bit 1 of 0.2 MUF is equal to:

$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4)\ \overline{U8} +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4) \cdot \overline{U8} +$$
$$T1 \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} + U2 \cdot \overline{U4} + \overline{U2} \cdot U4) \cdot \overline{U8} +$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} \cdot U4)$$

Bit 4 of 0.3 x MUF is equal to:

$$T4 + T1 \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + U8) + T1 \cdot T2 \cdot (\overline{U1} + \overline{U2}) +$$
$$T1 \cdot T2 \cdot (U1 + U2)\ (\overline{U4} \cdot \overline{U8}) +$$
$$T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + \overline{T1} \cdot T2 \cdot (\overline{U1} + \overline{U2})$$

Bit 3 of 0.3 x MUF is equal to:

$$T4 + T1 \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + U8) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$T1 \cdot \overline{T2}\ (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + T1 \cdot \overline{T2}\ (\overline{U1} + \overline{U2}) +$$
$$T1 \cdot \overline{T2} \cdot (U1 + U2)\ (\overline{U4} \cdot \overline{U8})$$

Bit 2 of 0.3 x MUF is equal to:

$$T1 \cdot T2 \cdot (\overline{U1} + \overline{U2}) + T1 \cdot T2 \cdot (U1 + U2)\ (\overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2\ (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4 + U8) + \overline{T1} \cdot \overline{T2} \cdot (\overline{U1} \cdot U2 \cdot U4)$$

Bit 1 of 0.3 x MUF is equal to:

$$T1 \cdot T2 \cdot (\overline{U1} + \overline{U2}) + T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + T1 \cdot \overline{T2} \cdot (\overline{U1} + \overline{U2})$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4 + U8) +$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} \cdot U4)$$

The detailed logic diagram which shows the generation of 0.1 x MUF, 0.2 x MUF, and 0.3 x MUF is shown in Figure 39.

In like manner, the equations for the bits of 0.5 x MUF can be written: Bit 5 of 0.5 x MUF is equal to:

$$T4 + T1 \cdot T2 \cdot (U1 \cdot U8) +$$
$$T1 \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot U4 + \overline{U1} \cdot U2 \cdot U4) +$$
$$T1 \cdot T2 \, (U1 \cdot U2 \cdot \overline{U4} + \overline{U1} \cdot \overline{U2} \cdot U4) +$$
$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4})$$

Bit 4 of 0.5 x MUF is equal to:

$$T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U2 \cdot \overline{U4} + \overline{U1} \cdot \overline{U2} \cdot U4) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U8)$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + T1 \cdot \overline{T2} \cdot (U1 \cdot U8)$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$T1 \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8)$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot U2 \cdot U4 + U1 \cdot \overline{U2} \cdot U4) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot U2 \cdot U4 + U1 \cdot \overline{U2} \cdot U4)$$

Bit 3 of 0.5 x MUF is equal to:

$$T1 \cdot T2 \cdot (U1 \cdot U8) + T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8})$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U2 \cdot \overline{U4} + \overline{U1} \cdot \overline{U2} \cdot U4) + \overline{T1} \cdot T2 \cdot (U1 \cdot U8)$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot U2 \cdot U4 + U1 \cdot \overline{U2} \cdot U4) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot U4 + U1 \cdot U2 \cdot \overline{U4}) +$$

$$T1 \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + \overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U8) +$$
$$\overline{T1} \cdot \overline{T2} \cdot (\overline{U1} \cdot U8)$$

Bit 2 of 0.5 x MUF is equal to:

$$T1 \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$T1 \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot U4 + \overline{U1} \cdot U2 \cdot U4) +$$
$$T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U8) + \overline{T1} \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8})$$
$$T1 \cdot \overline{T2} \cdot (U1 \cdot U8) + \overline{T1} \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8)$$
$$\overline{T1} \cdot T2 \cdot (\overline{U1} \cdot U2 \cdot U4 + U1 \cdot \overline{U2} \cdot U4) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot U4 + U1 \cdot U2 \cdot \overline{U4}) +$$
$$T1 \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}) +$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4)$$
$$\overline{T1} \cdot \overline{T2} \cdot (\overline{U1} \cdot U2 \cdot U4)$$

Bit 1 of 0.5 x MUF is equal to:

$$T1 \cdot T2 \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot U4 + U1 \cdot U2 \cdot \overline{U4})$$
$$T1 \cdot T2 \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8} + \overline{U1} \cdot U2 \cdot \overline{U4}) +$$
$$\overline{T1} \cdot T2 \cdot (U1 \cdot U8) + T1 \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4 + \overline{U1} \cdot U8) +$$
$$T1 \cdot \overline{T2} \cdot (\overline{U1} \cdot \overline{U2} \cdot \overline{U4} \cdot \overline{U8}) + \overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U8)$$
$$\overline{T1} \cdot \overline{T2} \cdot (U1 \cdot U2 \cdot U4) + \overline{T1} \cdot \overline{T2} \cdot (U1 \cdot \overline{U2} \cdot U4)$$

The logic diagram for the 0.5 x MUF board is shown in Figure 40.

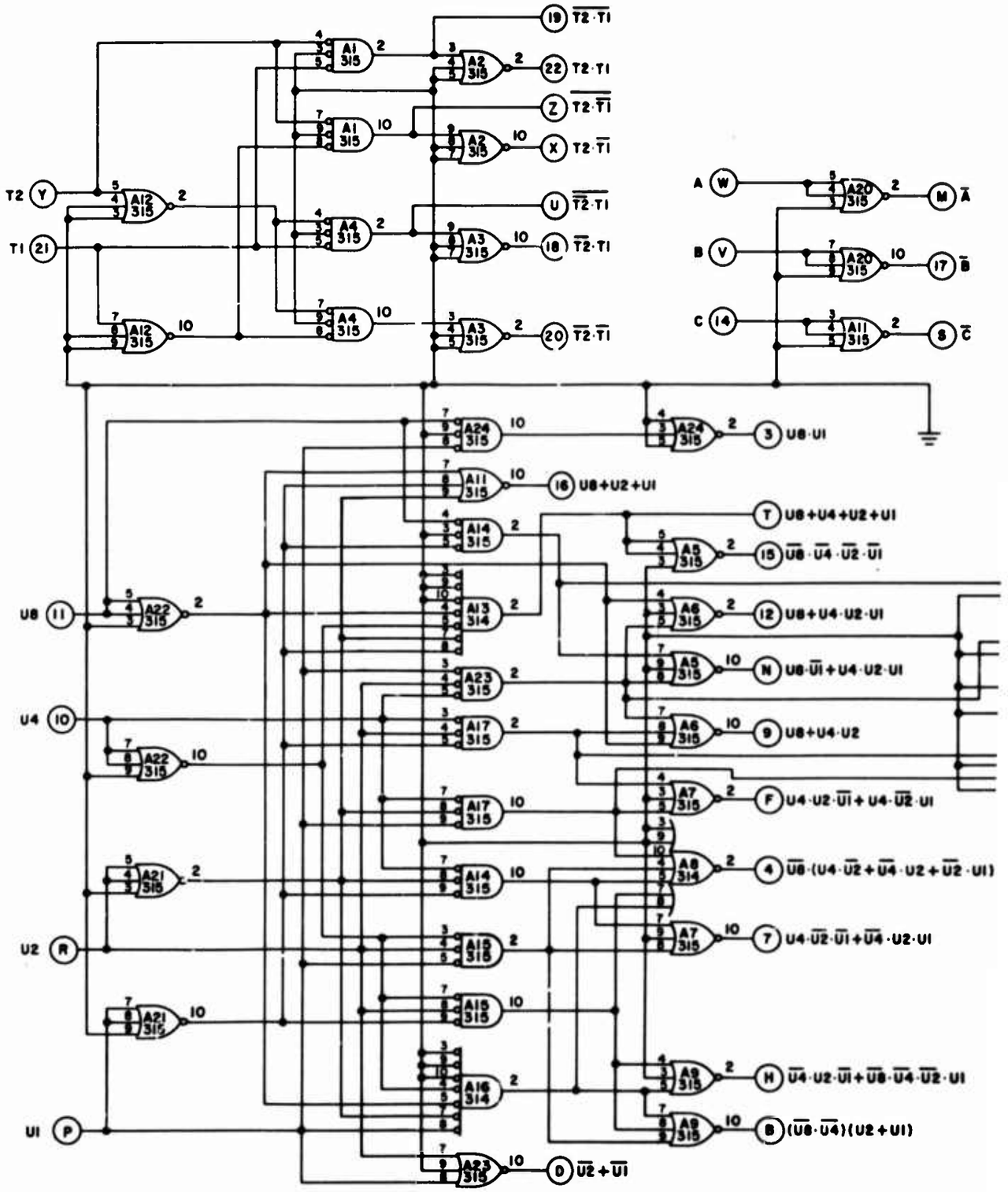

T2 Y
T1 21
U8 11
U4 10
U2 R
U1 P
A W
B V
C 14
19 $\overline{T2 \cdot T1}$
22 T2·T1
Z $\overline{T2 \cdot \overline{T1}}$
X T2·$\overline{T1}$
U $\overline{\overline{T2} \cdot T1}$
18 $\overline{T2}$·T1
20 $\overline{T2 \cdot T1}$
M $\overline{A}$
17 $\overline{B}$
S $\overline{C}$
3 U8·U1
16 U8+U2+U1
T U8+U4+U2+U1
15 $\overline{U8 \cdot U4 \cdot U2 \cdot U1}$
12 U8+U4·U2·U1
N U8·$\overline{U1}$+U4·U2·U1
9 U8+U4·U2
F U4·U2·$\overline{U1}$+U4·$\overline{U2}$·U1
4 $\overline{U8}$·(U4·$\overline{U2}$+$\overline{U4}$·U2+$\overline{U2}$·U1)
7 U4·$\overline{U2}$·$\overline{U1}$+$\overline{U4}$·U2·U1
H $\overline{U4}$·U2·$\overline{U1}$+$\overline{U8}$·$\overline{U4}$·$\overline{U2}$·U1
B ($\overline{U8}$·$\overline{U4}$)(U2+U1)
D $\overline{U2}$+$\overline{U1}$

Figure 38.

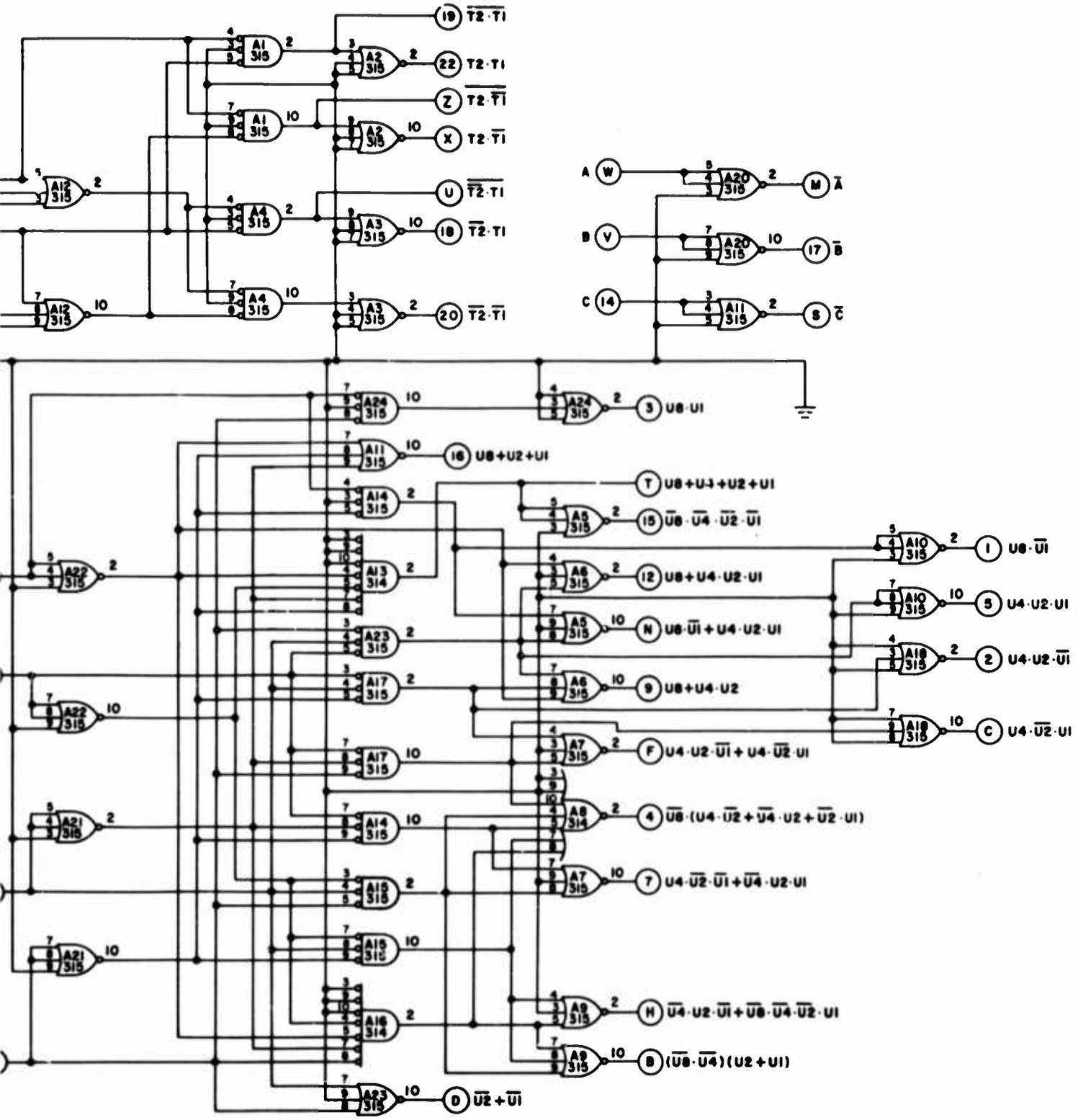
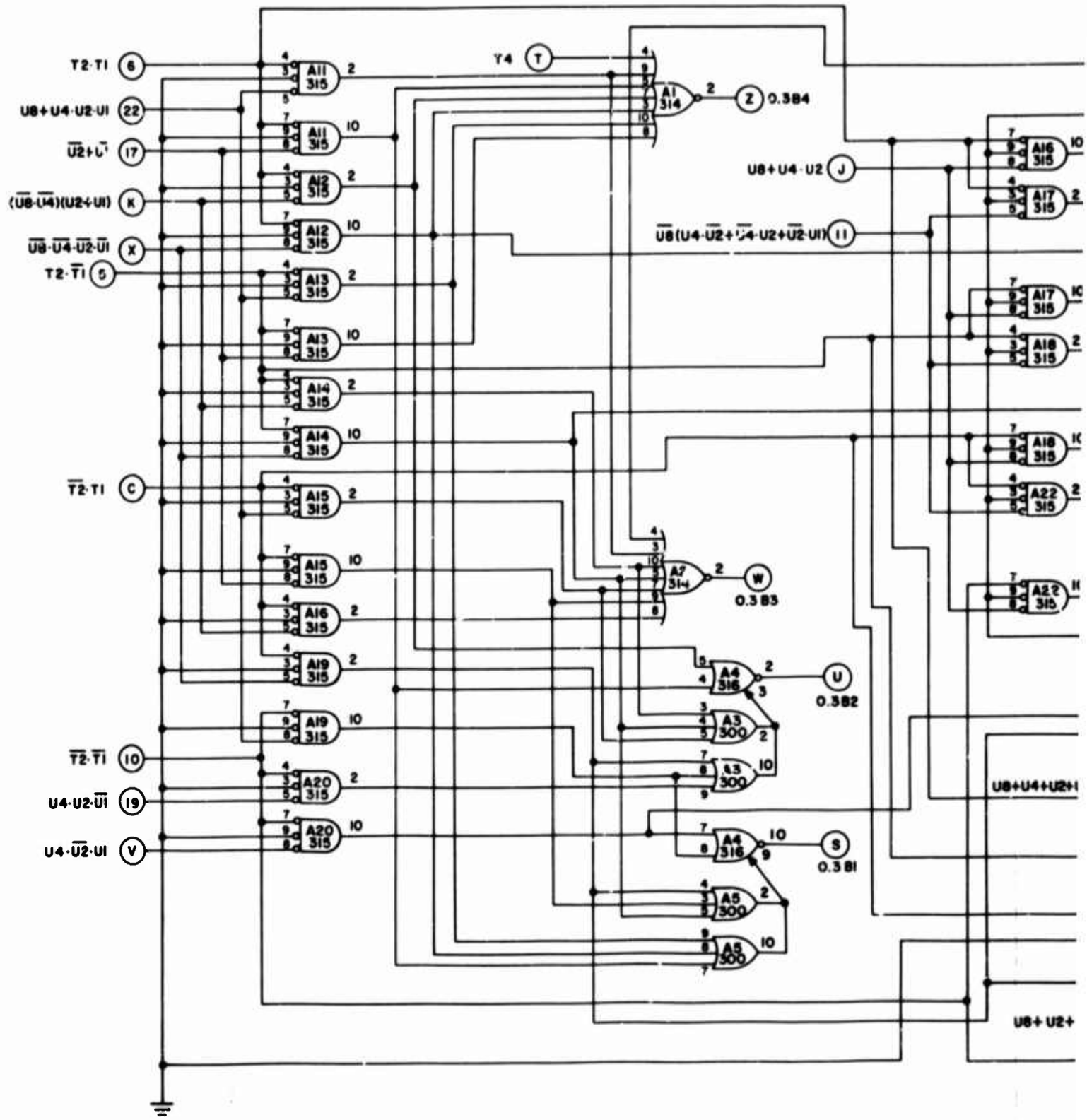


Figure 38. MUF Fraction Logic

2


T2·T1
6
U8+U4·U2·U1
22
U2+U1
17
(U8·U4)(U2+U1)
K
U8·U4·U2·U1
X
T2·T1
5
T2·T1
C
T2·T1
10
U4·U2·U1
19
U4·U2·U1
V
Y4
T
A11 315
A11 315
A12 315
A12 315
A13 315
A13 315
A14 315
A14 315
A15 315
A15 315
A16 315
A19 315
A19 315
A20 315
A20 315
A1 314
Z
0.384
U8+U4·U2
J
U8(U4·U2+U4·U2+U2·U1)
11
A7 314
W
0.383
A4 316
U
0.382
A3 300
A3 300
A4 316
S
0.381
A5 300
A5 300
A16 315
A17 315
A17 315
A18 315
A18 315
A22 315
A22 315
U8+U4+U2+
U8+U2+

1

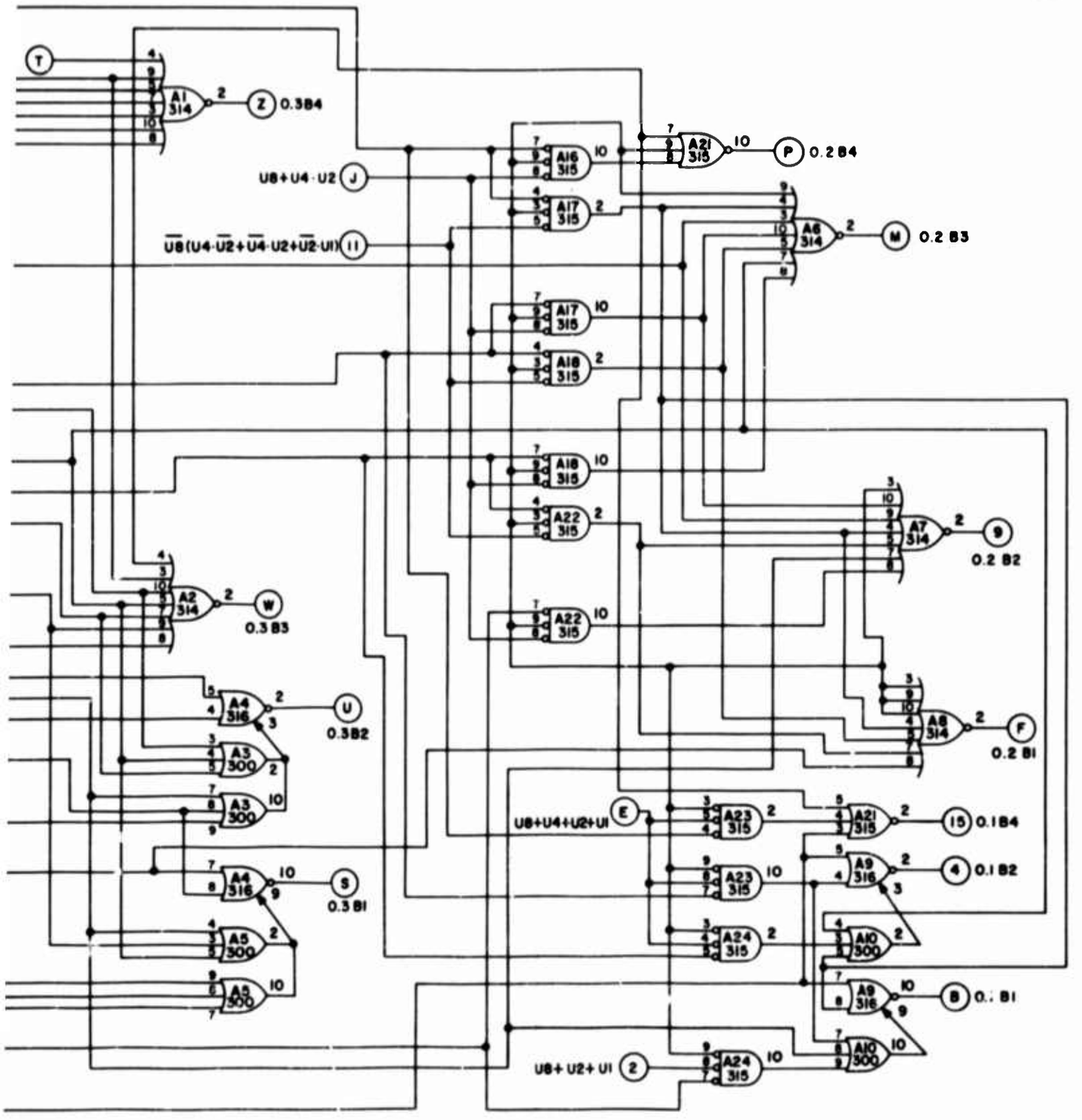
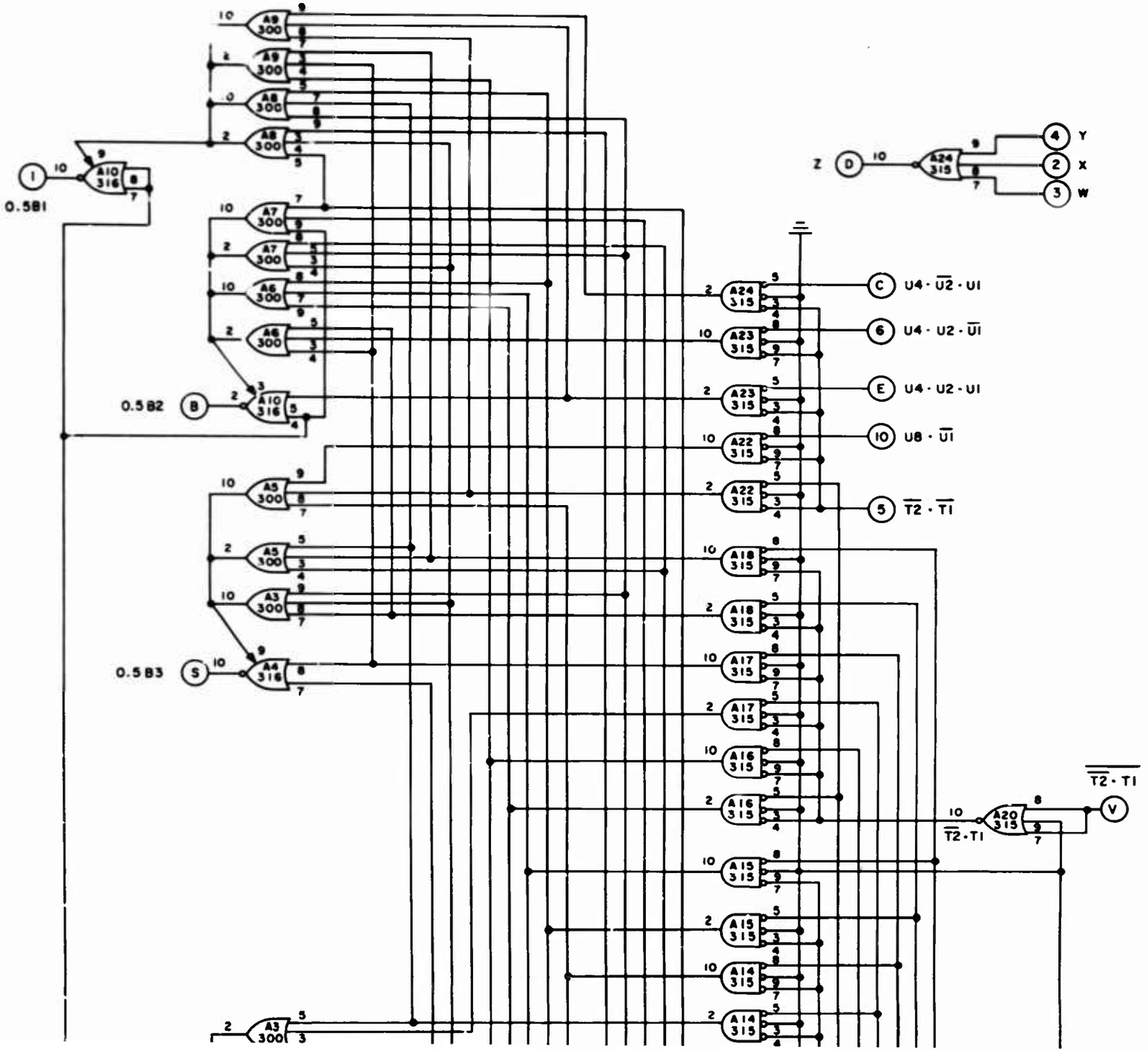


Figure 39. MUF Fractions (0.1, 0.2, 0.3)


0.581
0.582
0.583
Z
Y
X
W
U4 · $\overline{U2}$ · U1
U4 · U2 · $\overline{U1}$
U4 · U2 · U1
U8 · $\overline{U1}$
$\overline{T2}$ · $\overline{T1}$
$\overline{T2 \cdot T1}$
$\overline{T2}$ · T1

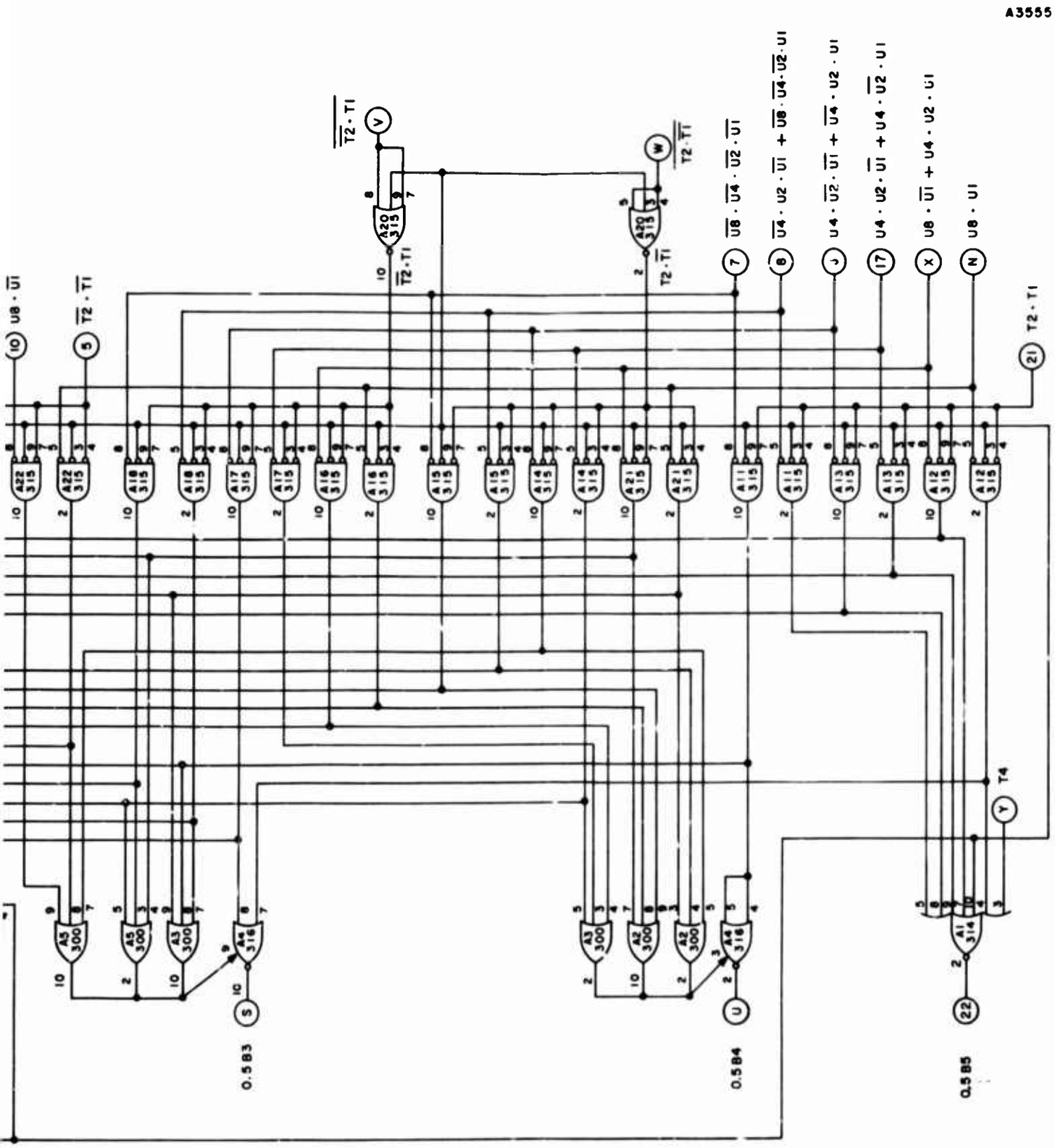


Figure 40. MUF Fraction (0.5)

c. Adder Gate

The binary numbers representing 0.1 x MUF, 0.2 x MUF, 0.3 x MUF, and 0.5 x MUF are put into a digital multiplexer gate. The multiplexer control inputs determine which fractional value of the MUF will be gated through the multiplexer. The multiplexer output is inverted so that outputs MF1 through MF5 represent the 1's complement of the fractional value of the MUF.

d. Adder

The logic described below is shown in Figure 37. Outputs MF1 through MF5 form one set of inputs, representing a fractional multiple of MUF, to a six-bit parallel adder. The other set of adder inputs is controlled by the output of the gate shown in Figure 36. In the N/I automatic mode this output is a binary number representing the MUF. A carry is forced into the first adder stage. The adder output is then equal to the MUF plus the one's complement of some fractional multiple of the MUF plus one. The one's complement of a number plus one is equal to the two's complement, or minus the number; therefore, the number at the adder output is equal to the MUF minus the selected fractional portion of the MUF.

e. RF Filter Selection

Three decode gates are used to decode the values of the adder outputs from 4 to 39. The decoder outputs control IF4 (interface circuits) which controls the relays that select the RF filters. In addition, OR gate 30ϭ-J senses whether the number out of the adder is equal to or greater than 22 and activates the upper relay. If the number out of the adder is less than 22 it activates the lower relay.

f. IF Control

The IF is related to the receiver RF as shown in Table XIV. The RF out of the adder is decoded to give the IF control lines. The following equations are implemented by the IF switching board (Figure 41).

$$7 = F + \overline{B}\overline{C}\overline{E}\overline{F} + CDE + B\overline{C}\overline{D}E + \overline{A}\overline{B}CD$$

$$19 = BD\overline{E} + \overline{B}\overline{D}E + B\overline{C}D + \overline{B}\overline{C}E + C\overline{D}E + AC\overline{D}\overline{F}$$

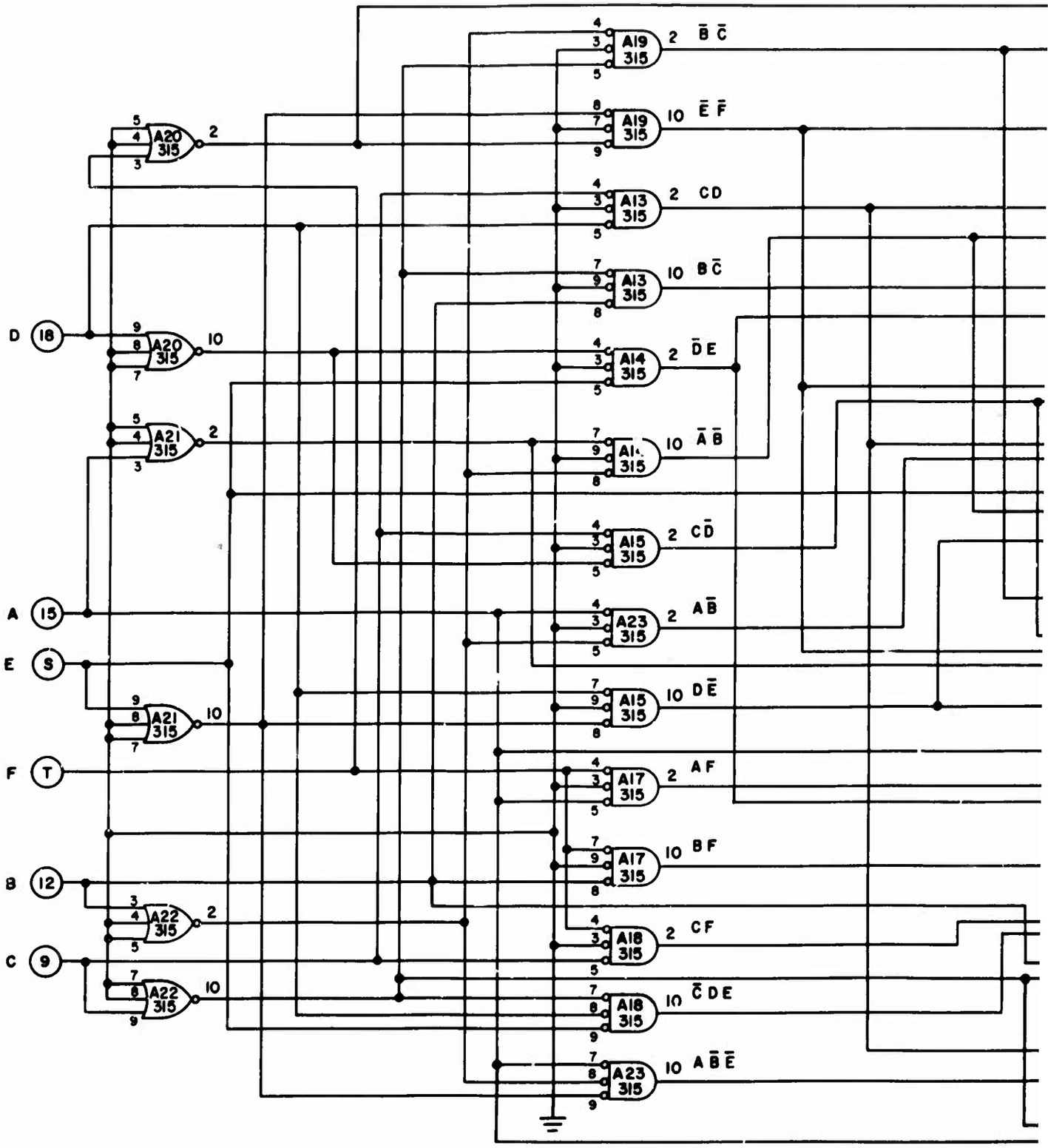
$$29 = \overline{A}C\overline{D}\overline{E}\overline{F} + A\overline{B}CD\overline{E}$$

On the logic diagram (Figure 36), the board inputs A, B, C, D, E, and F are called F MON 1, F MON 2, F MON 3, F MON 4, F MON 5, and F MON 6, respectively.

TABLE XIV

TRUTH TABLE, RF TO IF

RF (MHz)	Synthesizer Frequency (MHz)	IF (MHz)	F MON 1 A	F MON 2 B	F MON 3 C	F MON 4 D	F MON 5 E	F MON 6 F
39	46	7	1	1	1	0	0	1
38	45	7	0	1	1	0	0	1
37	44	7	1	0	1	0	0	1
36	43	7	0	0	1	0	0	1
35	42	7	1	1	0	0	0	1
34	41	7	0	1	0	0	0	1
33	40	7	1	0	0	0	0	1
32	39	7	0	0	0	0	0	1
31	38	7	1	1	1	1	1	0
30	37	7	0	1	1	1	1	0
29	36	7	1	0	1	1	1	0
28	35	7	0	0	1	1	1	0
27	46	19	1	1	0	1	1	0
26	45	19	0	1	0	1	1	0
25	44	19	1	0	0	1	1	0
24	43	19	0	0	0	1	1	0
23	42	19	1	1	1	0	1	0
22	41	19	0	1	1	0	1	0
21	40	19	1	0	1	0	1	0
20	39	19	0	0	1	0	1	0
19	26	7	1	1	0	0	1	0
18	25	7	0	1	0	0	1	0
17	36	19	1	0	0	0	1	0
16	35	19	0	0	0	0	1	0
15	34	19	1	1	1	1	0	0
14	33	19	0	1	1	1	0	0
13	42	29	1	0	1	1	0	0
12	19	7	0	0	1	1	0	0
11	30	19	1	1	0	1	0	0
10	29	19	0	1	0	1	0	0
9	16	7	1	0	0	1	0	0
8	15	7	0	0	0	1	0	0
7	26	19	1	1	1	0	0	0
6	35	29	0	1	1	0	0	0
5	24	19	1	0	1	0	0	0
4	33	29	0	0	1	0	0	0


A19 315
2 $\bar{B}\,\bar{C}$
A19 315
10 $\bar{E}\,\bar{F}$
A20 315
2
A13 315
2 CD
A13 315
10 $B\bar{C}$
D 18
A20 315
10
A14 315
2 $\bar{D}E$
A21 315
2
A14 315
10 $\bar{A}\,\bar{B}$
A15 315
2 $C\bar{D}$
A 15
A23 315
2 $A\bar{B}$
E 5
A21 315
10
A15 315
10 $D\bar{E}$
F T
A17 315
2 AF
A17 315
10 BF
B 12
A22 315
2
A18 315
2 CF
C 9
A22 315
10
A18 315
10 $\bar{C}\,DE$
A23 315
10 $A\bar{B}\bar{E}$

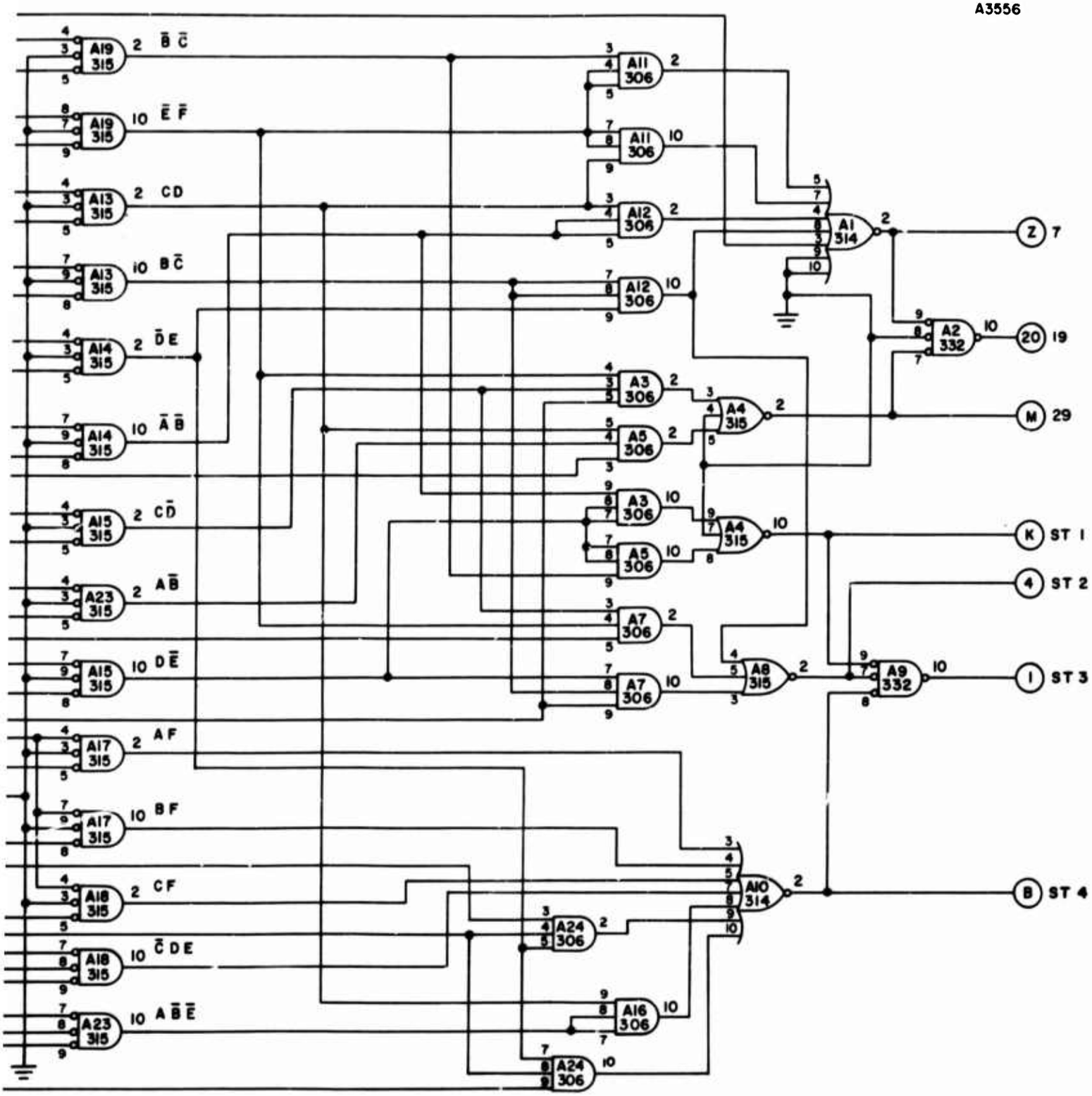


Figure 41. IF Switching Logic

g. Synthesizer Control

(1) Megahertz Digits Control

The 10-MHz and unit-MHz digits of the synthesizer frequency are a function of the RF, as shown in Table XIV. Logic on the IF switching board (Figure 41) also decodes the adder output to control the 10-MHz digit of the synthesizer. The following equations are implemented:

$$ST1 = \overline{A}\ \overline{B}\ D\ \overline{E} + \overline{B}\ \overline{C}\ D\ \overline{E}$$

$$ST2 = B\ \overline{C}\ \overline{D}\ E + A\ C\ \overline{D}\ \overline{E}\ \overline{F} + \overline{A}\ B\ \overline{C}\ D\ \overline{E}$$

$$ST3 = B\ C\ D + A\ B\ D\ \overline{E} + \overline{A}\ C\ \overline{D}\ \overline{E}\ \overline{F} + C\ D\ E + \overline{A}\ \overline{B}\ \overline{D}\ E + \overline{A}\ \overline{B}\ \overline{C}\ F + \overline{B}\ \overline{C}\ \overline{D}\ E$$

$$ST4 = AF + BF + CF + \overline{C}\ D\ E + A\ \overline{B}\ C\ D\ \overline{E} + B\ C\ \overline{D}\ E + A\ C\ \overline{D}\ E$$

External logic is used to sense that ST1, ST2, ST3, and ST4 are all absent, which is equivalent to making the 10-MHz digit zero.

The units-MHz digit control lines for the synthesizer are generated by OR'ing together the appropriate decoded adder outputs.

(2) Automatic Kilohertz Digits Control

Figure 42 shows the logic that controls the 100-kHz, 10-kHz, and 1-kHz digits of the synthesizer in the N/I automatic mode.

A 10-stage ring counter is used to control each kHz digit of the synthesizer. The output of each counter is encoded to provide a BCD code representing the value of the digit. The three ring counters have a common reset and a common clock. When the counter is reset, all 10 stages of each counter will be reset. When preparing to use the ring counters in the N/I automatic mode, flip-flop XA411-9 will cause the first stage of each ring counter to be set. This is equivalent to putting zero into each counter. After data are taken at a particular frequency, four pulses are counted in the kHz ring counter (since data are taken in 4-kHz increments). Each time the 1-kHz counter reaches 9, it enables itself to be set to zero on the next pulse and allows one count to be added to the 10-kHz counter. When nine exists in the 1-kHz and 10-kHz counters, the 10-kHz counter is enabled to go to zero and one count is added to the 100-kHz ring counter.

The logic that controls the kHz ring counters will now be described. Flip-flops XA311, XA312, and XA313 control the initialization of the kHz counters. Flip-flops XA314 and XA315 sense the fact that the digital processor has completed a reading. Flip-flop

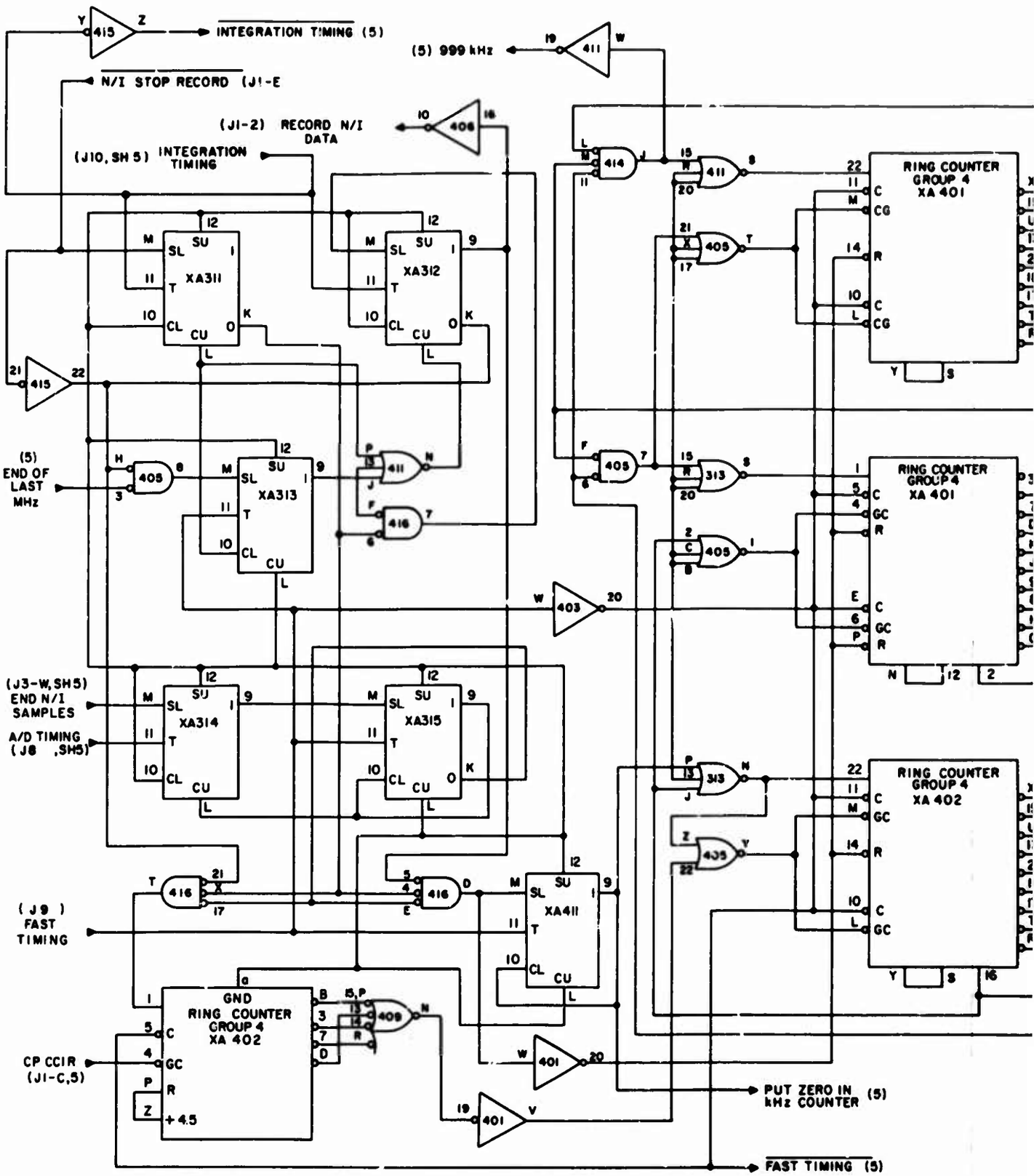
XA411 actually zeros the ring counter. Ring counter XA402 allows four counts to be added to the kHz counter.

If we assume that the N/I record stop switch is operated at the control panel, XA311 and XA312 are reset through the CU inputs and flip-flop XA313 is set at the SU input. If the operator now depresses the record start switch at the control panel, flip-flop XA311 will be set by the next integration timing (0.3-, 3.0-, or 300-second) pulse. Flip-flops XA311 and XA313 are now in the one state, and flip-flop XA312 is in the zero state. When flip-flop XA314 senses that the receiver output has been sampled, it will be set to the one state. This in turn causes XA315 to be set to the one state at the next clock time. This, combined with XA311 being in the one state and XA312 being in the zero state, will reset the kHz counters and enable flip-flop XA411.

The next clock pulse will set flip-flop XA411. The next clock pulse will cause zero to be placed in the kHz counter and reset XA411. At the end of the integration period XA312 will be set to the one state. When XA312 is in the one state data are accumulated in the digital processor. Now when XA314 senses an end of sample, the ring counter XA402-B causes four counts to be inserted into the kHz counters. Data will stop being accumulated if the last megahertz has been processed or if the operator depresses the N/I stop record switch at the control panel.

(3) Kilohertz Multiplexer Gate

The kHz digits of the synthesizer are controlled from five sources. In the automatic mode of operation they are controlled by the 3-kHz ring counters. In the manual mode of operation they are controlled from the thumbwheel switches at the N/I receiver digital control cabinet. In the CCIR mode the 1-kHz digit only is controlled from three thumbwheel switches at the N/I control panel. All of these signals exist in BCD form. The signals are fed into a digital multiplexer. The multiplexer output is decoded to provide the needed 10 control lines for each decade. The multiplexer gate is shown in Figure 43.


INTEGRATION TIMING (5)
(5) 999 kHz
N/I STOP RECORD (J1-E
(J1-2) RECORD N/I DATA
(J10, SH 5) INTEGRATION TIMING
RING COUNTER GROUP 4 XA 401
RING COUNTER GROUP 4 XA 401
RING COUNTER GROUP 4 XA 402
(5) END OF LAST MHz
(J3-W, SH5) END N/I SAMPLES
A/D TIMING (J8 ,SH5)
(J9) FAST TIMING
CP CCIR (J1-C,5)
GND
RING COUNTER GROUP 4 XA 402
+4.5
PUT ZERO IN kHz COUNTER (5)
FAST TIMING (5)

1

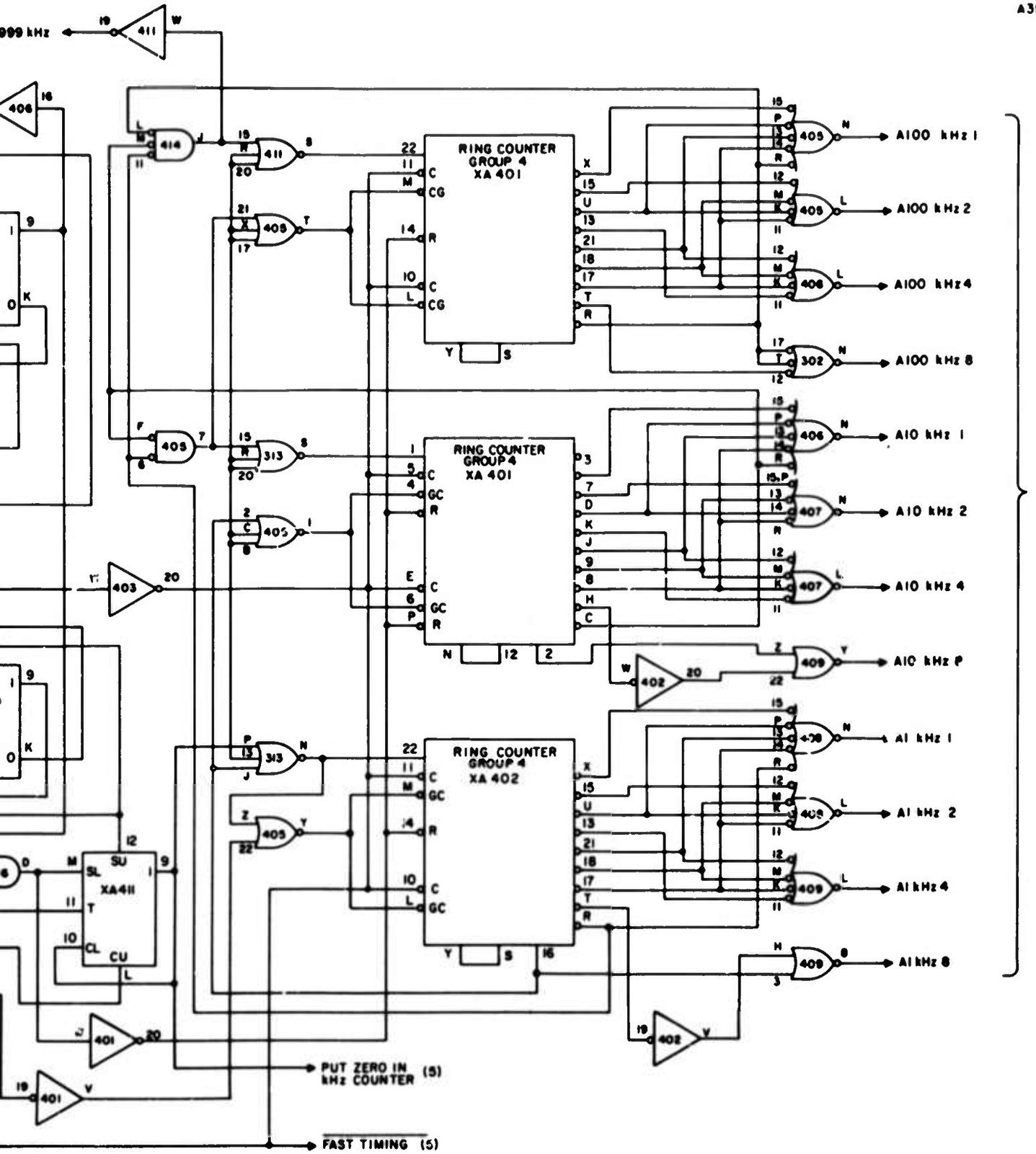
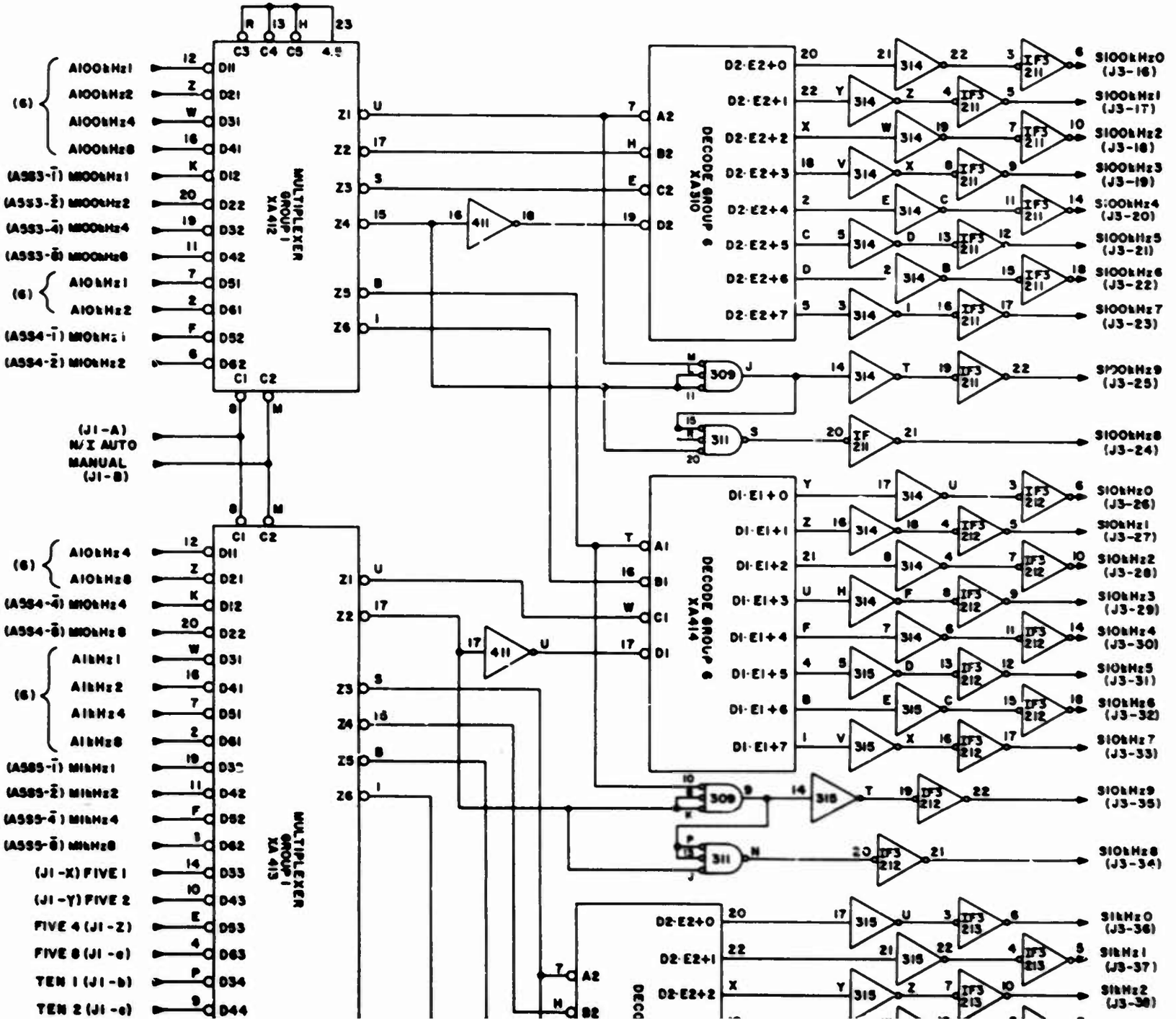


Figure 42. Kilohertz Digits Control


MULTIPLEXER GROUP I XA 412
MULTIPLEXER GROUP I XA 413
DECODE GROUP 6 XA310
DECODE GROUP 6 XA414
DECODE GROUP 6
(6) A100kHz1
A100kHz2
A100kHz4
A100kHz8
(A583-1) M100kHz1
(A583-2) M100kHz2
(A583-4) M100kHz4
(A583-8) M100kHz8
(6) A10kHz1
A10kHz2
(A584-1) M10kHz1
(A584-2) M10kHz2
(J1-A) N/I AUTO MANUAL (J1-B)
(6) A10kHz4
A10kHz8
(A584-4) M10kHz4
(A584-8) M10kHz8
(6) A1kHz1
A1kHz2
A1kHz4
A1kHz8
(A585-1) M1kHz1
(A585-2) M1kHz2
(A585-4) M1kHz4
(A585-8) M1kHz8
(J1-X) FIVE 1
(J1-Y) FIVE 2
FIVE 4 (J1-Z)
FIVE 8 (J1-e)
TEN 1 (J1-b)
TEN 2 (J1-c)
D2·E2+0
D2·E2+1
D2·E2+2
D2·E2+3
D2·E2+4
D2·E2+5
D2·E2+6
D2·E2+7
D1·E1+0
D1·E1+1
D1·E1+2
D1·E1+3
D1·E1+4
D1·E1+5
D1·E1+6
D1·E1+7
S100kHz0 (J3-16)
S100kHz1 (J3-17)
S100kHz2 (J3-18)
S100kHz3 (J3-19)
S100kHz4 (J3-20)
S100kHz5 (J3-21)
S100kHz6 (J3-22)
S100kHz7 (J3-23)
S100kHz9 (J3-25)
S100kHz8 (J3-24)
S10kHz0 (J3-26)
S10kHz1 (J3-27)
S10kHz2 (J3-28)
S10kHz3 (J3-29)
S10kHz4 (J3-30)
S10kHz5 (J3-31)
S10kHz6 (J3-32)
S10kHz7 (J3-33)
S10kHz9 (J3-35)
S10kHz8 (J3-34)
S1kHz0 (J3-36)
S1kHz1 (J3-37)
S1kHz2 (J3-38)

Figure

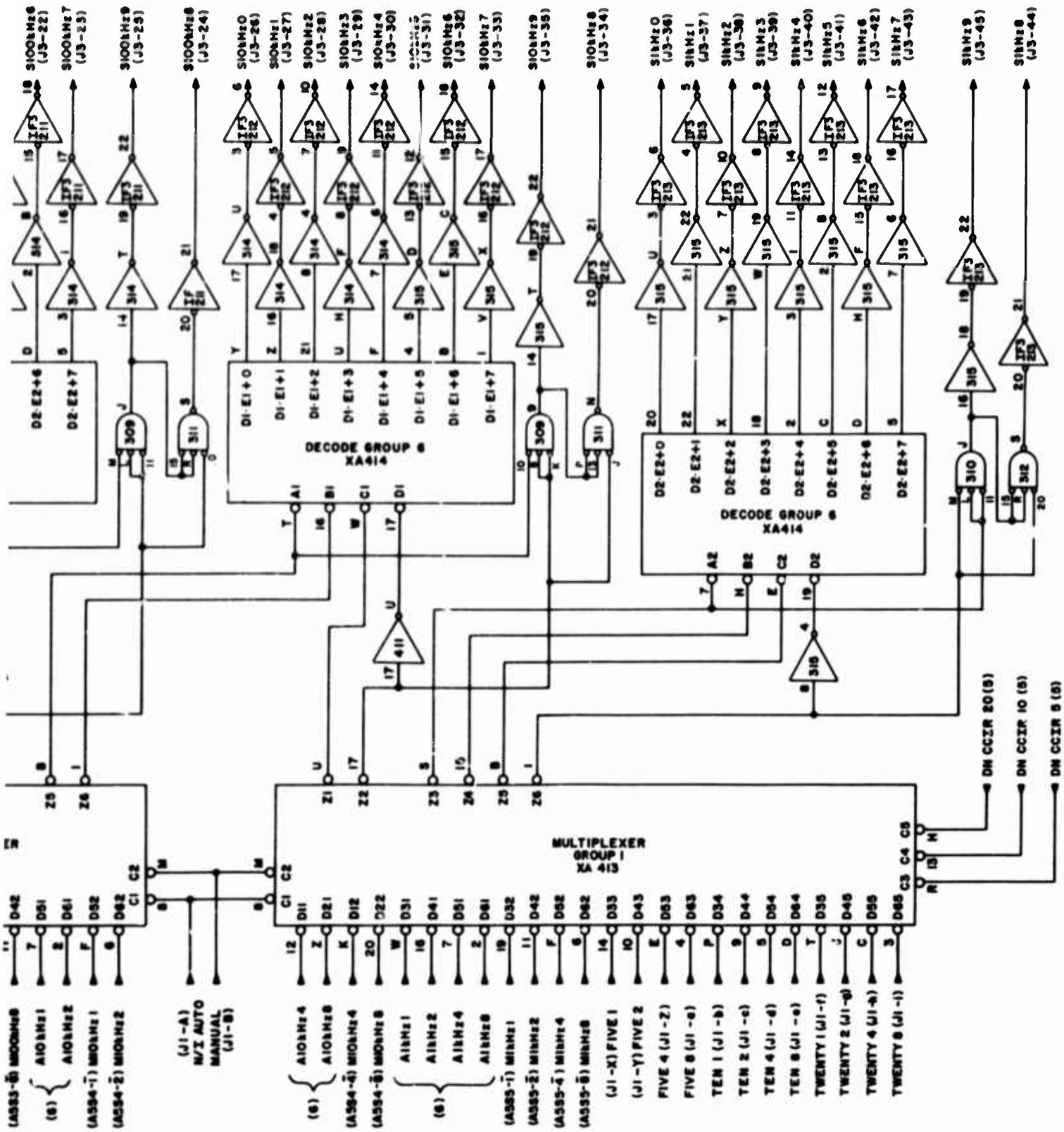


Figure 43. Kilohertz Multiplexer Gate

h. MUF Fraction Sequence Control Logic

These circuits (shown in Figure 44) select the correct fractional multiple of the MUF to gate through to the adder. The sequencing control is performed by a five-stage ring counter. The signal that allows zero to be placed in the kHz counters also enables this ring counter. When the first stage is set, it allows logic to sense whether the operator has selected the 1.0 MUF switch at the control panel. If the 1.0 MUF switch is not selected, the output of gate 406-20 is down, which advances the ring counter to the next state. In this way, MUF fractions not selected at the control panel are skipped. If the 1.0 MUF switch is selected, the output of logic gate 406-7 is up, which stops the ring counter and the outputs of logic gates 406-Y, 406-8, 407-7, and 407-Y are down. This causes no fraction to be gated through to the adder which is equivalent to subtracting zero from the MUF.

When the last reading for that frequency has been processed, as determined by the occurrence of the 999-kHz signal, the ring counter will be stopped until another selected fractional MUF switch is found. The last MUF fraction has been processed if the ring counter is in state 5 and 999 kHz occurs, or if the ring counter is in state 5 and the 0.5 x MUF switch is not selected at the MUF. This resets the kHz counter control logic and turns on a light at the control panel to tell the operator that the experiment is finished.

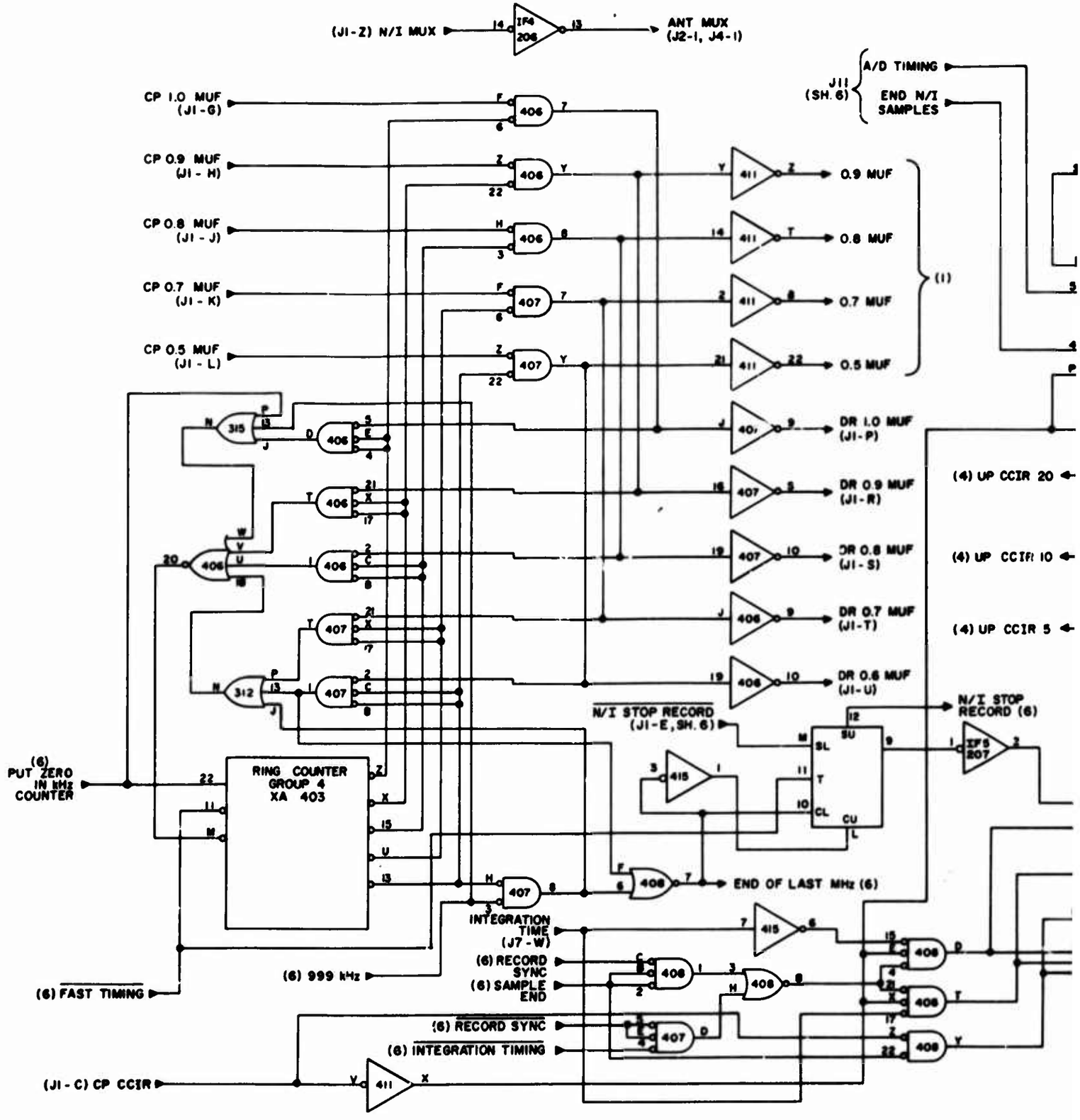
Also shown in Figure 44 is the logic that controls the selection of the CCIR frequency in the CCIR mode of operation. Again a ring counter performs the sequencing. If the CCIR mode is not selected the ring counter is reset and all three CCIR control lines are disabled. If the CCIR mode is selected, the fact that the first four stages are zeros will cause the first stage to be set to the one state the next time the digital processor has finished sampling the N/I receiver outputs. At this time, the three CCIR control lines are still disabled. During all succeeding sampling intervals, the ring counter will sequentially enable the 5-, 10-, and 20-MHz CCIR control lines until the operator deselects the CCIR mode switch. A two-bit code denoting the monitored CCIR frequency is recorded on magnetic tape.

i. Integrator Dump Logic

The integrators in the N/I receiver equipment need to be dumped (i.e., the capacitors in the integrating amplifiers must be discharged) at the beginning of each integration period. When data are being recorded, the end of the N/I receiver sampling process is sensed by gate 408-1 (shown in Figure 44). Gate 408-D will cause the 0.3 multivibrator to fire if we are not in the CCIR mode and the integration time is 0.3 second; the integrator dump signal will last approximately 3 ms. If we are not in the CCIR mode and the integration time is 3.0 seconds, gate 408-T will trigger the 3.0 multivibrator. This will cause an

integrator dump signal of approximately 30 ms. If data are not being recorded, the integrator dump signals will be initiated from an integration timing signal from the digital processor.

In the CCIR mode, logic gate 408-Y will trigger the 500 multivibrator which will generate an integrator dump signal of about three seconds.


(J1-Z) N/I MUX
IF4 206
ANT MUX (J2-1, J4-1)
A/D TIMING
J11 (SH. 6)
END N/I SAMPLES
CP 1.0 MUF (J1-G)
CP 0.9 MUF (J1-H)
CP 0.8 MUF (J1-J)
CP 0.7 MUF (J1-K)
CP 0.5 MUF (J1-L)
0.9 MUF
0.8 MUF
0.7 MUF
0.5 MUF
(1)
DR 1.0 MUF (J1-P)
DR 0.9 MUF (J1-R)
DR 0.8 MUF (J1-S)
DR 0.7 MUF (J1-T)
DR 0.6 MUF (J1-U)
(4) UP CCIR 20
(4) UP CCIR 10
(4) UP CCIR 5
N/I STOP RECORD (J1-E, SH. 6)
N/I STOP RECORD (6)
(6) PUT ZERO IN kHz COUNTER
RING COUNTER GROUP 4 XA 403
END OF LAST MHz (6)
INTEGRATION TIME (J7-W)
(6) 999 kHz
(6) RECORD SYNC
(6) SAMPLE END
(6) FAST TIMING
(6) RECORD SYNC
(6) INTEGRATION TIMING
(J1-C) CP CCIR

1

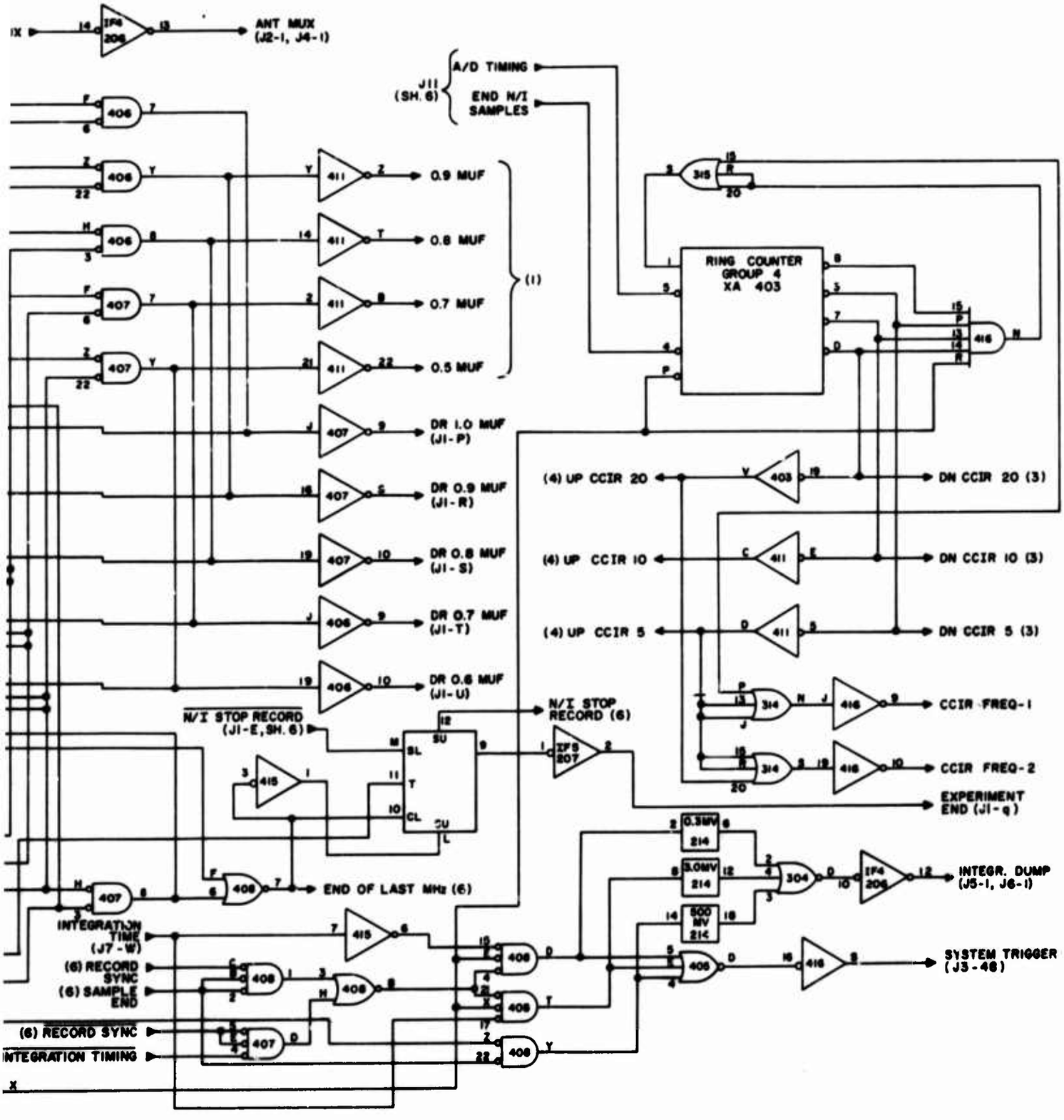


Figure 44. MUF Fraction Sequence Control Logic

j. Logic Boards

(1) IF3 Board

This board (shown in Figure 45) contains 10 circuits which translate logic levels of 0 and 4.5 volts to levels of -12.6 volts and open circuit. This circuit is used to interface with the Hewlett Packard synthesizer.

If the input is 0 volt, Q1 will be turned on. The collector of Q1 will rise toward 4.5 volts and turn on Q2. The collector of Q2 will be at -12.6 volts.

When the input is at 4.5 volts, no base current flows through Q1 which means that Q1 is turned off. This prevents base current from flowing through Q2. Q2 is turned off and the collector output will appear as an open circuit to the HP frequency synthesizer.

(2) IF4 Board

The IF4 board (shown in Figure 46) contains eight circuits which convert the 0- and 4.5-volt logic levels to 0- and 12-volt levels which drive relays in the receiver equipments.

When the input to the circuit is 0 volt, the output of the SE157K circuit is 4.5 volts, which turns on Q1. The collector of Q1 goes to ground and causes base current to flow through Q2, turning it on. The collector of Q2 will go to 12 volts which will operate control relays in the receiver equipments.

When the input to the circuit is 4.5 volts, the SE157K output is 0 volt and Q1 is turned off. This turns off Q2 which prevents the relay load from being driven.

(3) L1 Logic Board

This board (shown in Figure 47) contains the following logic elements:

2 three-input OR gates
14 inverters
1 flip-flop

(4) L2 Logic Board

This board (shown in Figure 48) contains the following logic elements:

3 three input NOR gates
3 two input NOR gates
1 five input AND gate
1 four input AND gate

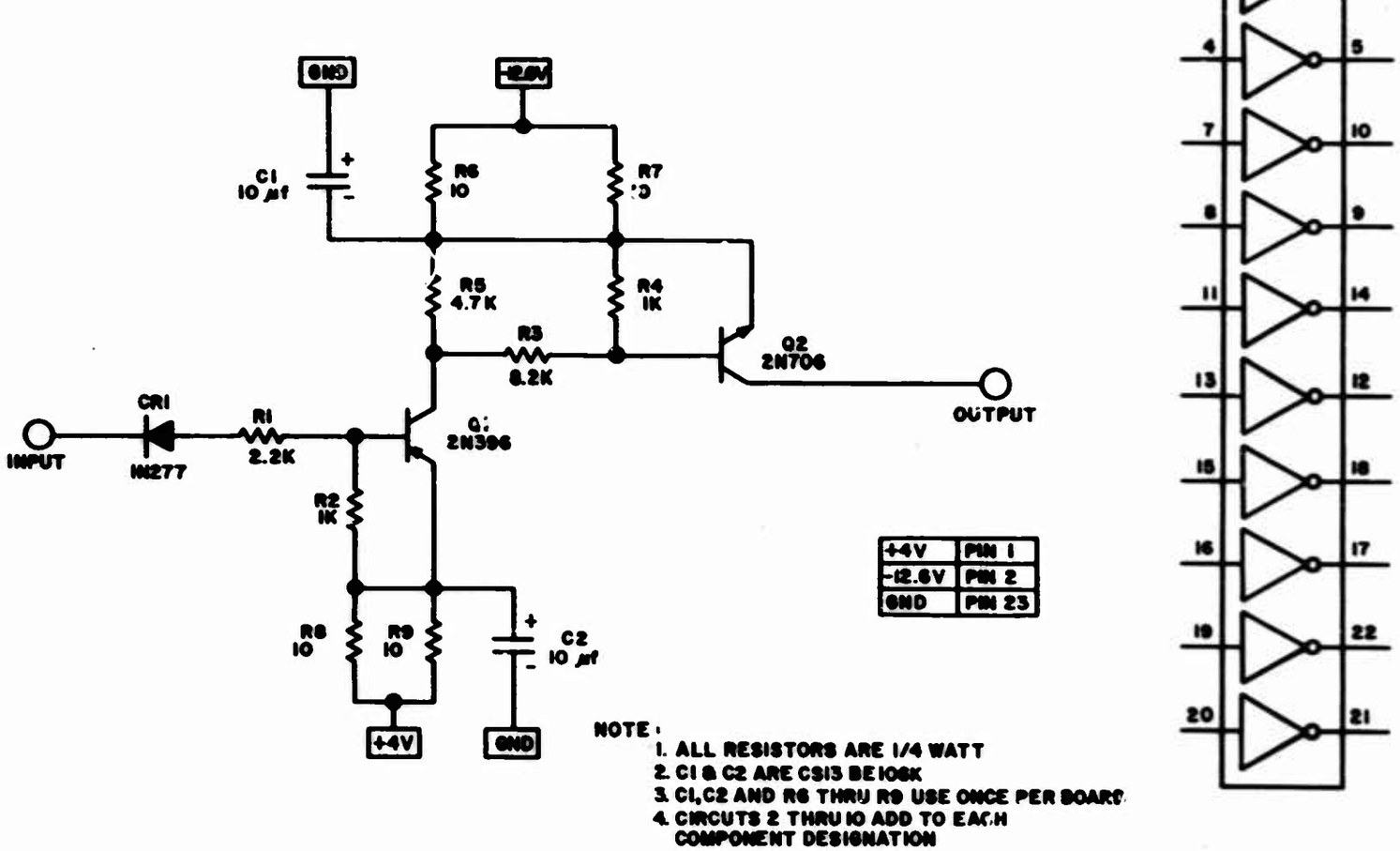


Figure 45. IF 3 Board

3 inverting line drivers

1 four input NOR gate

(5) MV, Multivibrator Board

This board (shown in Figure 49) contains three single-shot multivibrators. When the 0.3 multivibrator is triggered it puts out a 3-ms pulse. When the 3.0 multivibrator is triggered it puts out a 30-ms pulse. When the 500 multivibrator is triggered it puts out a three-second pulse.

(6) IF5 Board

This board contains eight circuits which allow logic levels of 0 and 4.5 volts to control lights at the control panel.

The circuit (shown in Figure 50) is identical to the IF4 circuit with the last stage deleted. When Q1 is conducting, current will flow through the indicator. When Q1 is turned off, current is prevented from flowing through the indicator.

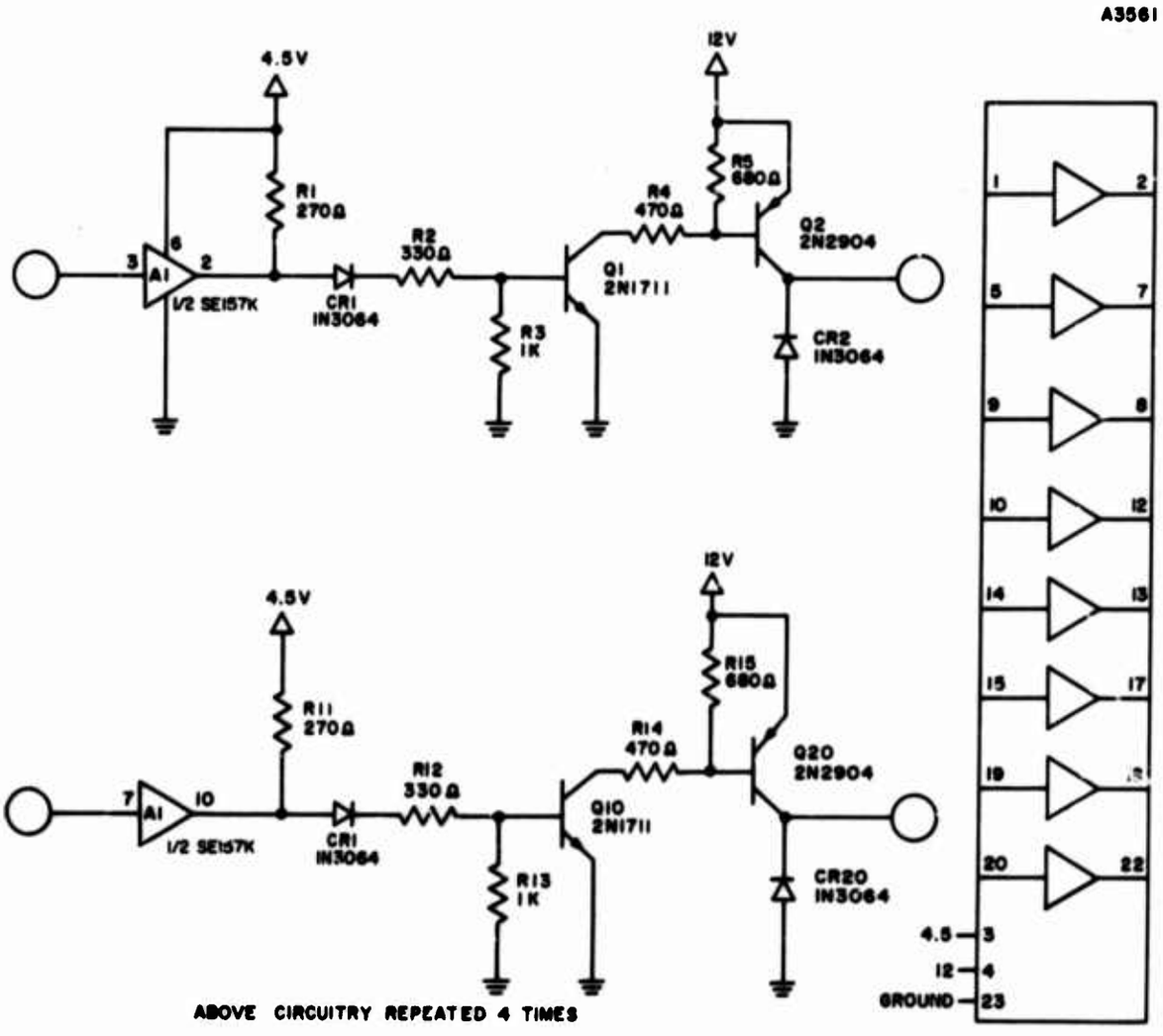


Figure 46. IF4 Board

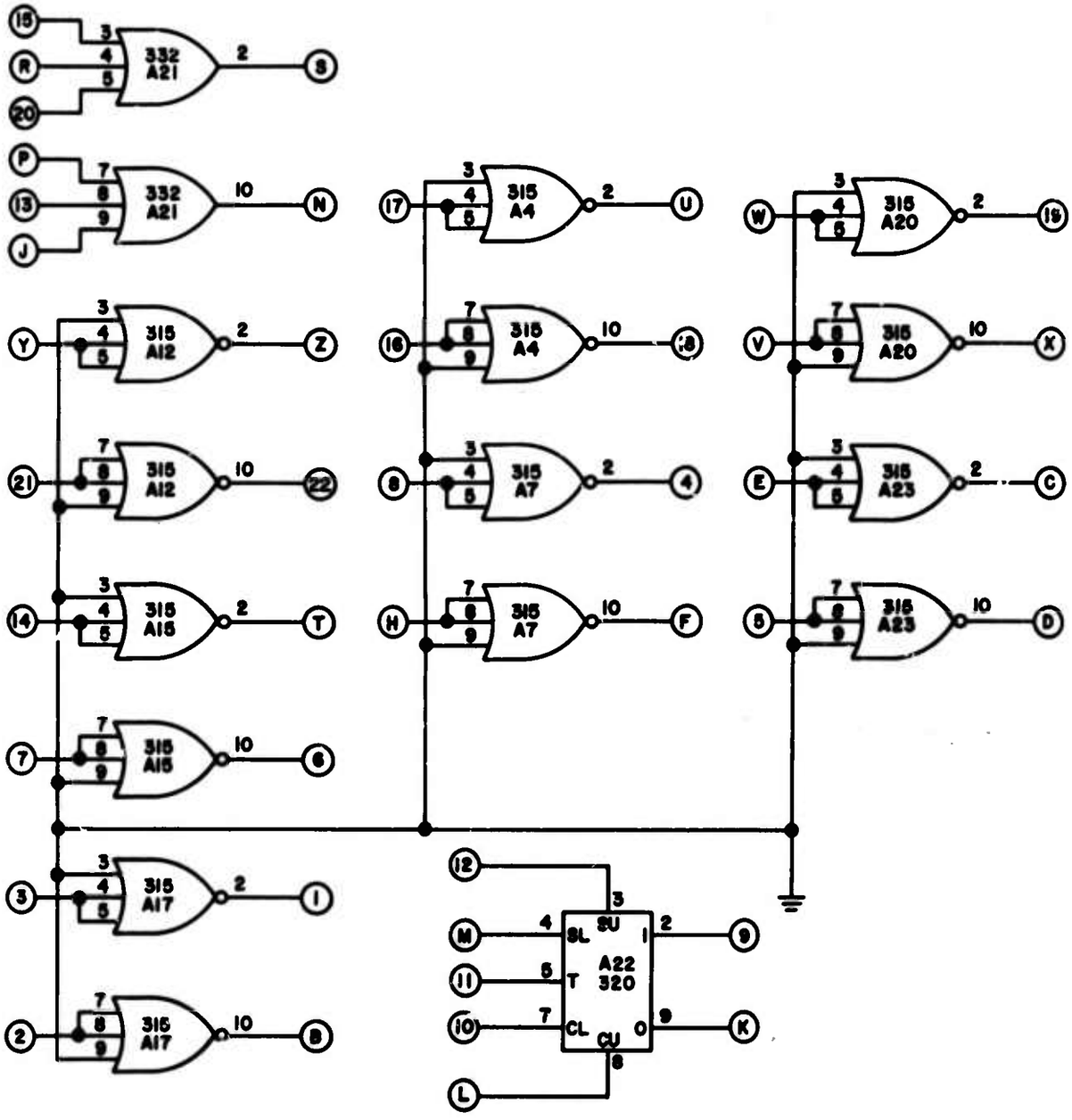


Figure 47. L1 Logic Board

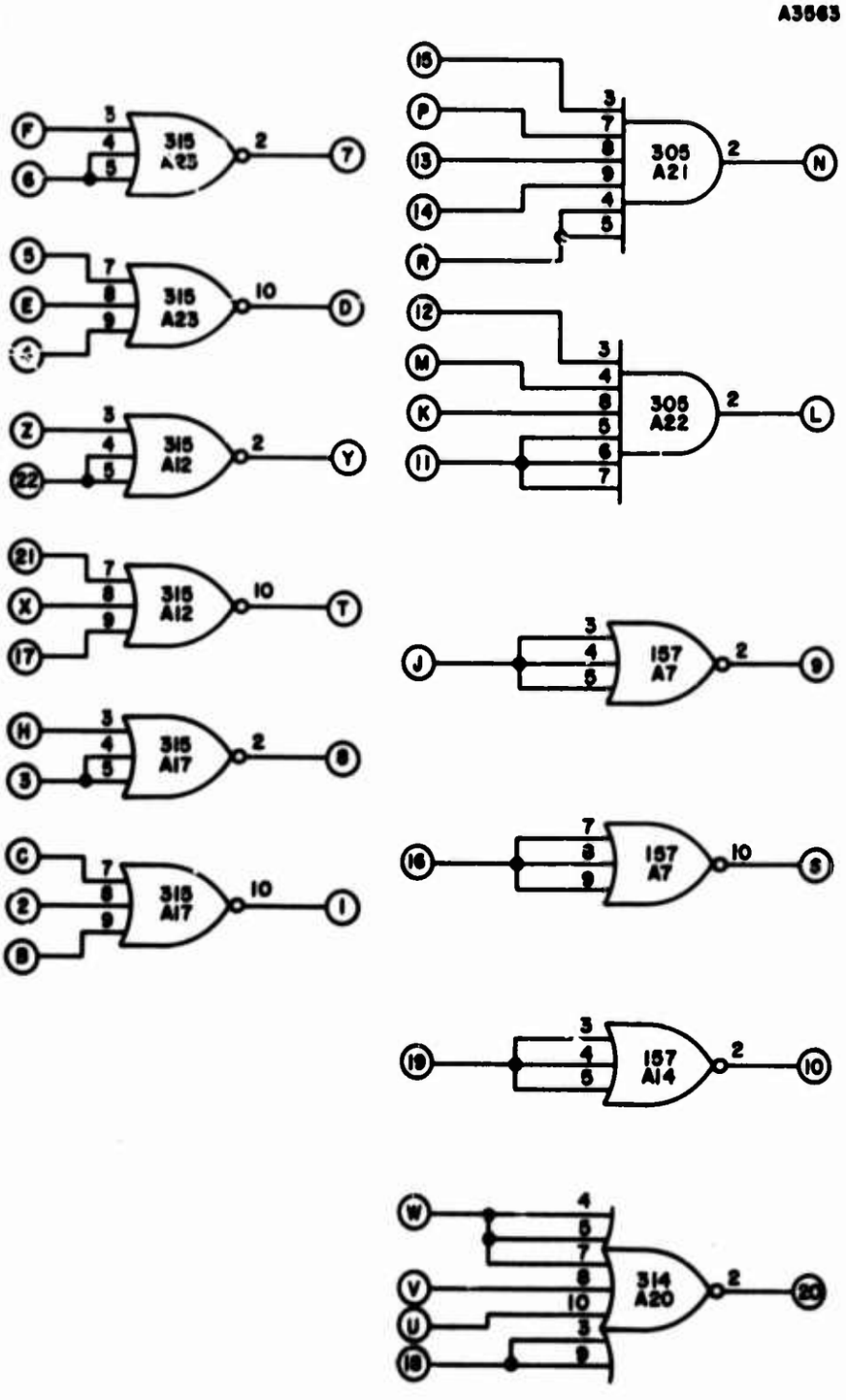


Figure 48. L2 Logic Board

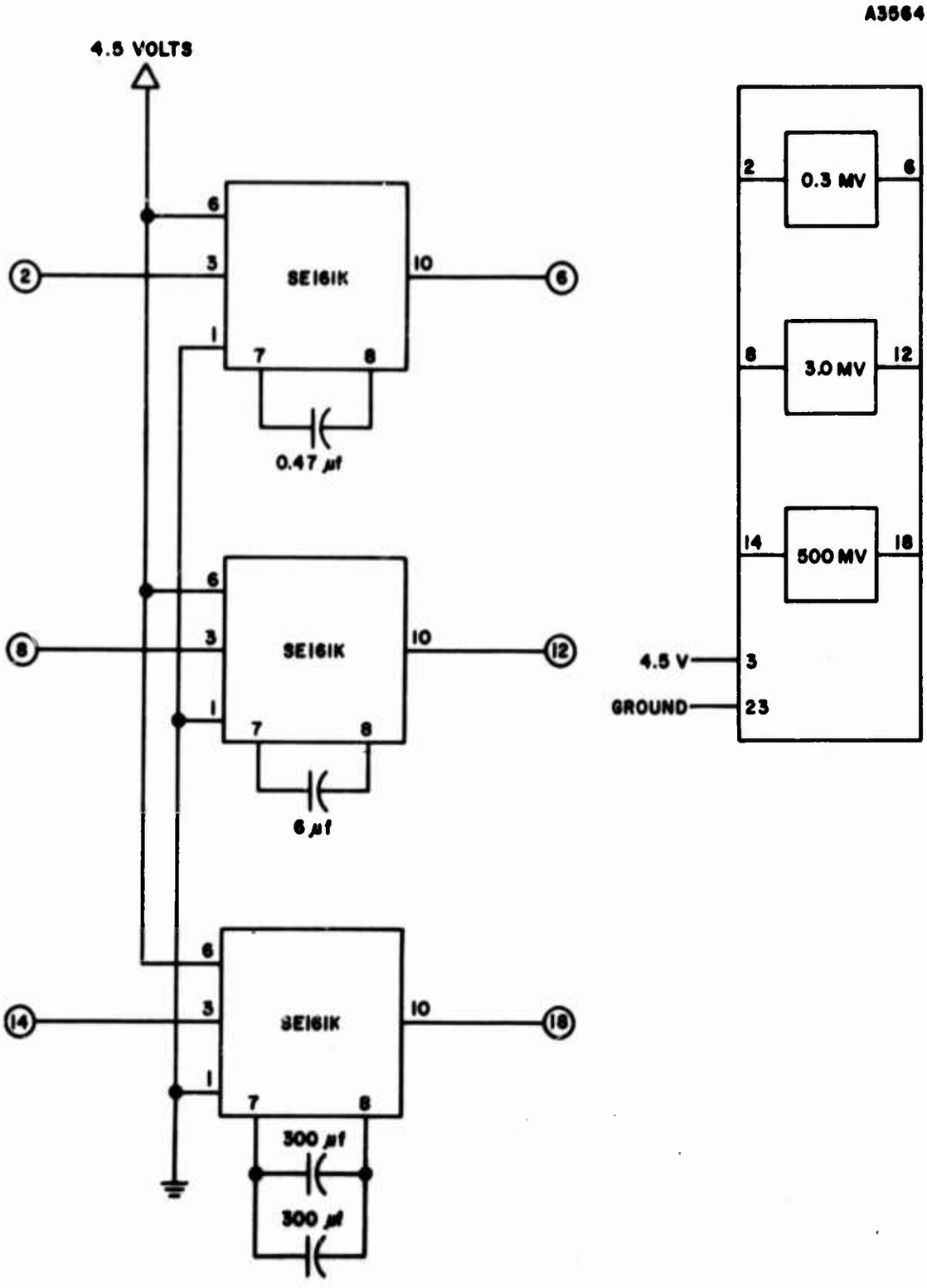


Figure 49. MV Board

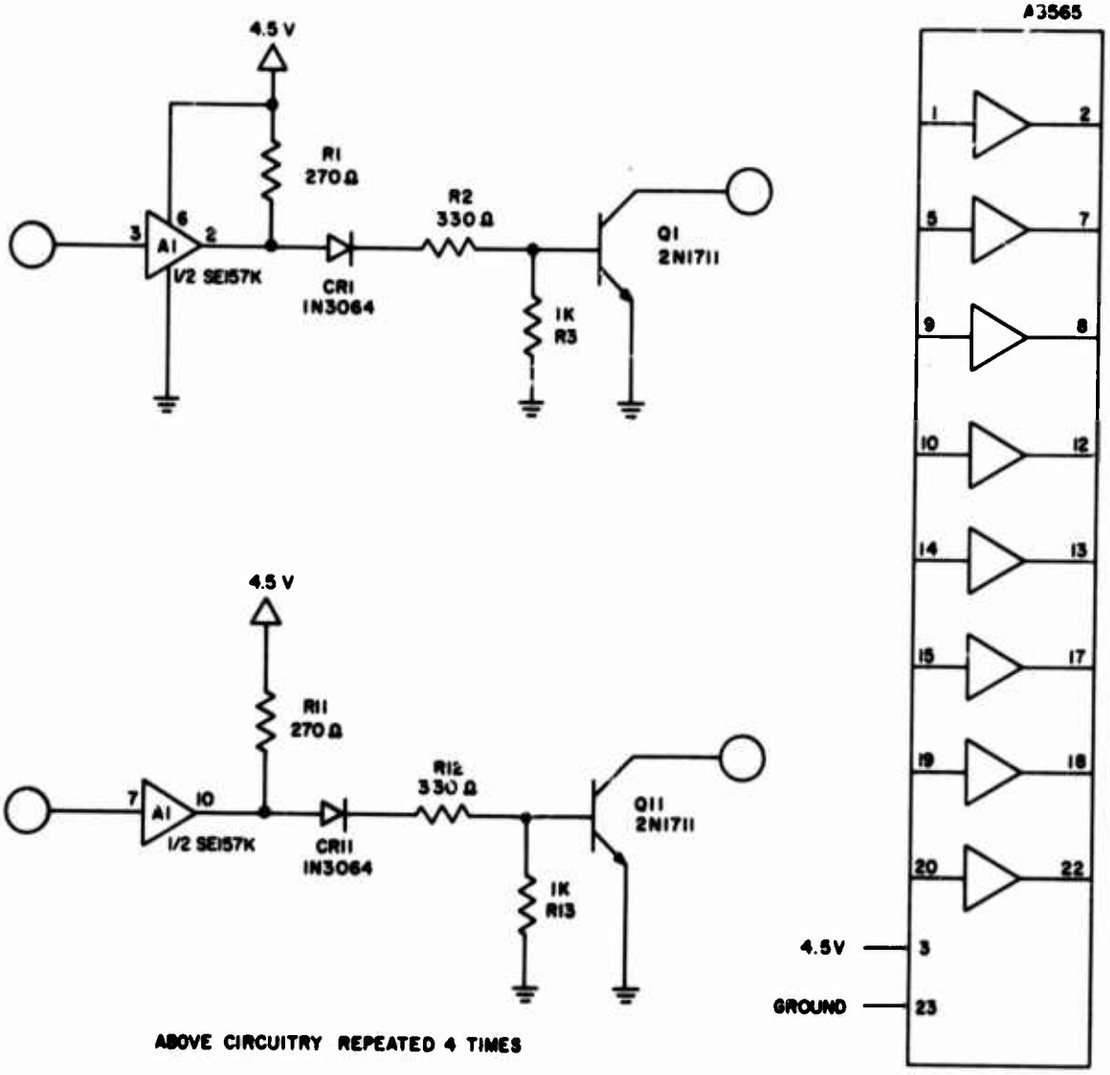


Figure 50. IF5 Board

SECTION IV

DIGITAL PROCESSOR

The basic function of the digital processor and the overall design and data formats are adequately discussed in Interim Report No. 1. This equipment has not yet been integrated into the system so that final drawings are not available. Therefore, a few unrelated topics which were not covered in the first report are discussed. A presentation of the complete logic diagrams is deferred until the final report. These topics include a discussion of the control panel, the time code generator interface, and a reporting of the format changes made since the last report.

1. CONTROL PANEL

The following controls are available to the operator on the mode loss/azimuth control panel shown in Figure 51.

a. Frequency

The frequency at which the mode loss/azimuth data are taken is set in by means of thumbwheel switches.

b. Calibration/Operate Mode Selection

The operator selects whether the equipment is in the calibrate or operate mode.

c. Recording Mode

The operator can choose to record data during the even 10-minute intervals, during the odd 10-minute intervals, and during all 10-minute intervals. In the above recording modes, data will be recorded during the last 8 minutes of the selected 10-minute interval. In the manual start recording mode, data will be recorded continuously starting with the next 40-second interval. The manual stop switch ends the recording of data.

d. Transmit Site

The operator indicates whether the north, east, or south site is transmitting.

e. Gate Adjust Potentiometers

These potentiometers control the positioning of gates over the received signal for each channel.

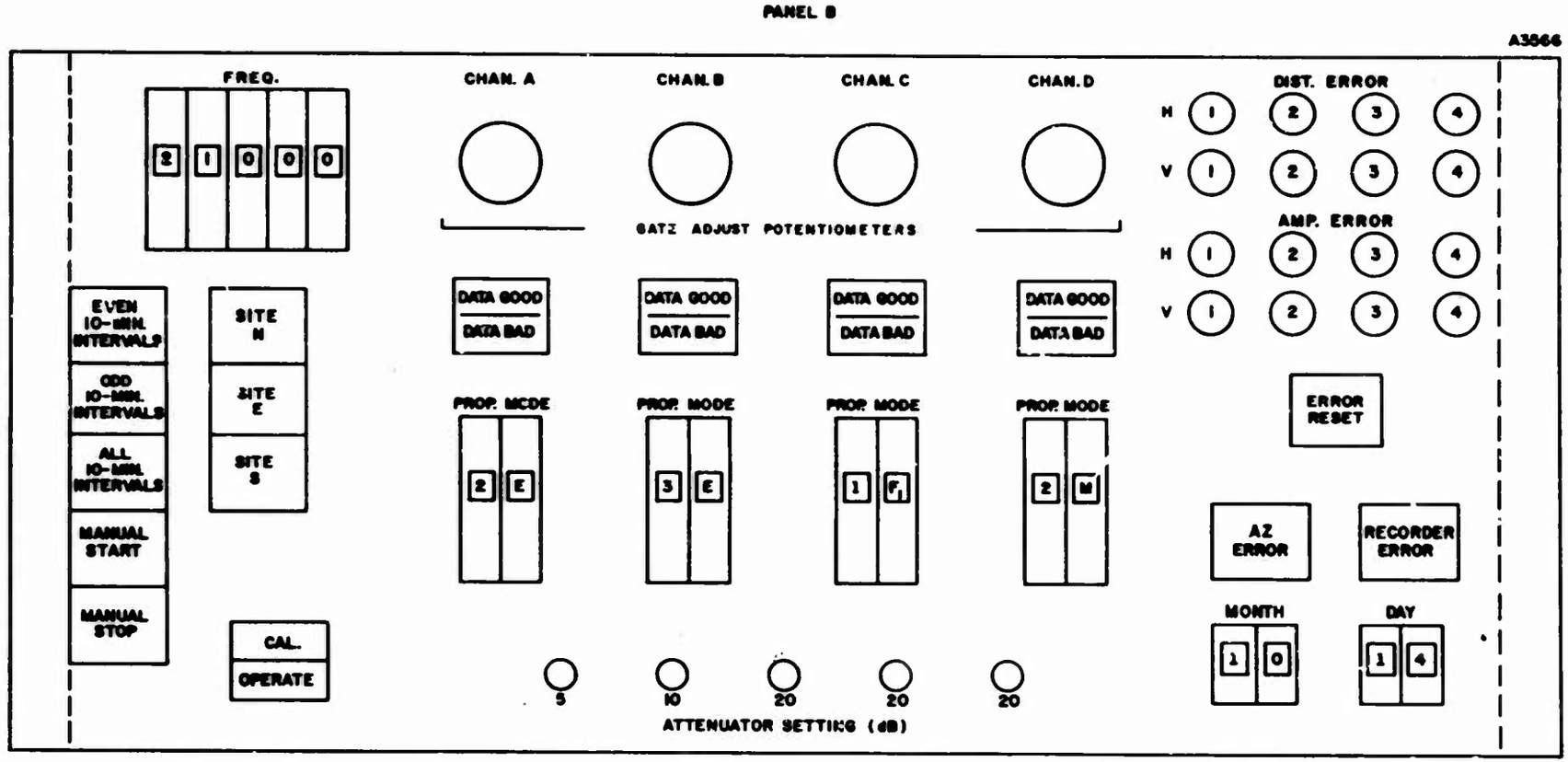


Figure 51. Digital Processor Control Panel

f. Data Good/Data Bad Switches

There is a data good/data bad switch for each channel. If the operator knows that data may not be valid in a channel (e.g., the received signal has drifted from under the gate) he indicates this. The states of the four switches are then recorded on magnetic tape.

g. Propagation Mode Switches

The operator can set in the propagation mode for each channel on thumbwheel switches. Two thumbwheel switches are used to designate the propagation mode for each channel. The first switch designates a number representing the number of hops. Although a number higher than three will probably never be selected, the switch can designate numbers up to seven. The second switch is used to denote the layer. The following selections are available: E, E_s, F1, F2, M, N; in addition, two blank positions are available on the switch for the operator to name special modes.

h. Attenuator Setting

The operator selects the amount of receiver attenuation (up to 75 dB in 5-dB steps).

i. Distribution and Amplitude Error Indicators

These are controlled from the digital processor and will be lit as soon as the signal in that channel exceeds the maximum that can be quantized by the A/D converter.

j. Error Reset Switch

When the operator presses this switch he will cause the distribution and amplitude error indicators to be reset.

k. Azimuth Error Indicator and Reset Switch

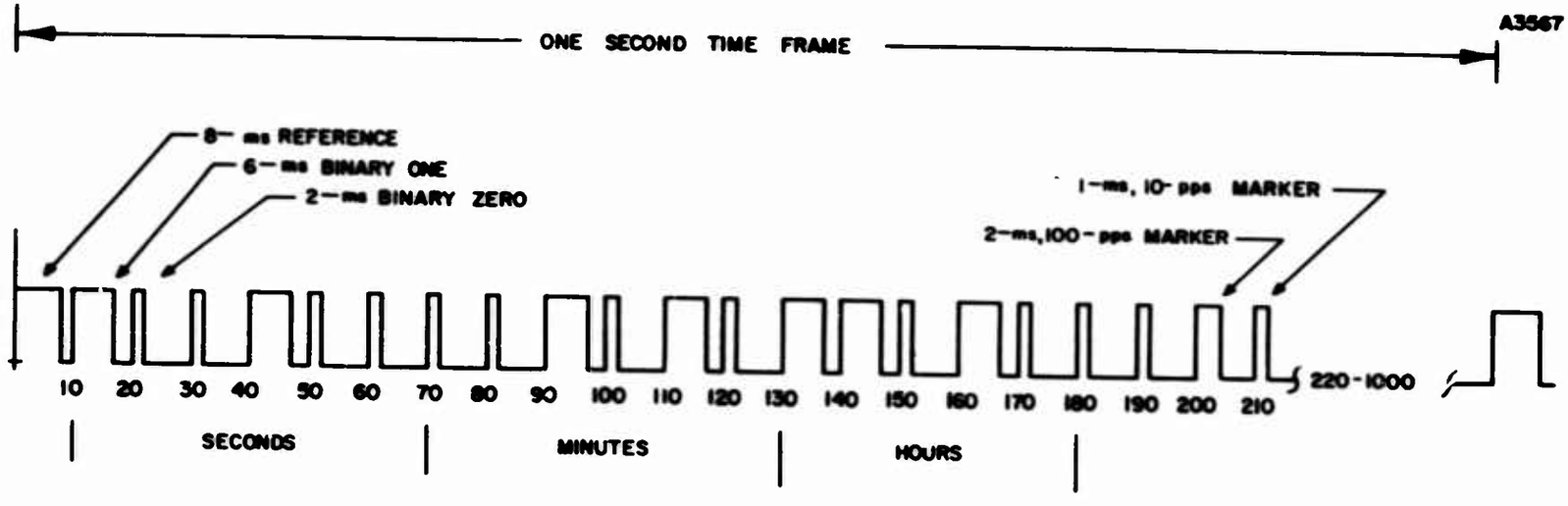
If any of the azimuthal angle of arrival signals exceed the maximum level, the azimuth error light is turned on. The light is reset when the operator hits the azimuth error indicating switch.

l. Recorder Error

This light will go on if there is a parity error generated by the magnetic tape unit.

m. Month and Day Switches

The operator sets in the day and month of the year which is recorded on magnetic tape.



TIME INDICATED IS 11 HOURS, 20 MINUTES, 9 SECONDS

Figure 52. AMR D-1 Time Code

2. TIME CODE GENERATOR INTERFACE

a. Function

This unit accepts timing signals from the Astrodata clock. It extracts the time of day from the time code signal for recording on magnetic tape. It also generates some of the timing signals required during the different experiments.

b. Inputs

(1) AMD1 Time Code

The time code is put out once every second (called a time frame) and consists of a reference mark, three subcode words of seconds, minutes, and hours, followed by 10- and 100-pps index markers (see Figure 52). The reference marker is an 8-ms pulse. The three subcode words consist of binary weighted pulses, with a 2-ms pulse representing a binary zero and a 6-ms pulse representing a binary one. The rest of the time frame is filled out with the 10-pps markers (represented by 4-ms pulses) and 100-pps markers (represented by 2-ms markers).

(2) 1000-pps Timing

This signal is used to extract the time information from the time code by measuring the duration of the pulses.

(3) 10-pps Timing Signal

This signal is used to generate 0.5-second timing signals.

c Outputs

The following signals are extracted from the time code and used by the digital processor.

(1) Time of Day

The time of day in hours, 10-minute intervals, and 40-second intervals is recorded on magnetic tape.

(2) Eight-Minute Gate

A gate marking the last 8 minutes of each 10-minute interval is generated which controls when mode loss data are taken.

(3) 39.5-Second Gate

This gate is used to sense the end of the 40-second data taking intervals.

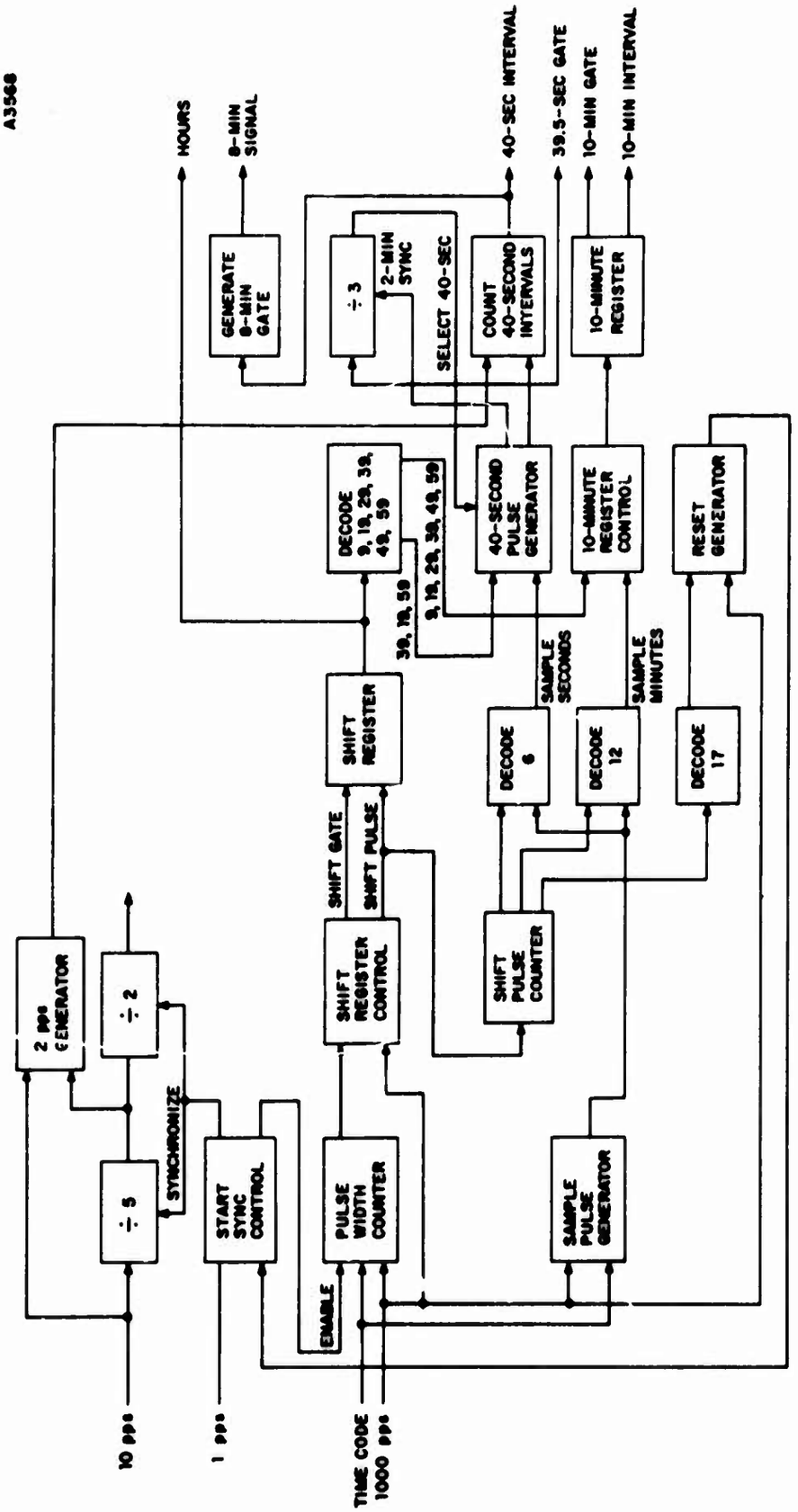


Figure 53. Timing Block Diagram

d. Design

The one pulse per second signal is used to start the processing of the time code information as shown in Figure 53. The pulse width counter is enabled. Using the 1000-pps signal, the width of each time code pulse is measured. After the pulse width is measured, a shift pulse is generated and value of the time code pulse (binary one or zero) is shifted into a six-bit shift register. A counter is used to keep track of the number of shift pulses that have been generated. After six shift pulses the seconds portion of the time code will exist in the shift register. Decode logic will sense whether the shift register contains 19, 39, or 59. A divide by 3 counter, synchronized by a 2-minute signal, will determine whether the end of a 40-second period is about to occur. The 40-second markers are counted in a binary counter and recorded on tape. The output of the 40-second counter is decoded to provide the 8-minute gate.

The time code continues to be fed into the shift register. When 12 shift pulses have been generated, the minutes portion of the time will exist in the shift register. If the time is the 59^{th} second and the number in the shift register is 9, 19, 29, 39, 49, or 59, then the binary number representing the number of 10-minute intervals since the hour began will be set into the 10-minute register.

The time code continues to be fed into the shift register. After the occurrence of the 17^{th} shift pulse, the hours portion of time will exist in the shift register. The hours portion of time is recorded on magnetic tape from the shift register.

3. FORMAT CHANGES

In order to facilitate the processing of data, the recording formats described in Interim Report No. 1 have been changed slightly. The only format that remains unchanged is the amplitude level data format. In all other formats the order in which characters have been recorded on tape has been changed. In addition, in the calibration format, four dummy characters have been inserted into the format. These changes are summarized below.

a. Mode Loss 10-Minute Header

The frequency information, characters 7 through 10, are recorded in the reverse order.

b. 40-Second Identification

The order of the two characters representing each gate time has been interchanged.

c. Amplitude, Azimuth, and Noise/Interference Distribution Data

The order of recording the two characters for each channel interval has been interchanged so that the six most significant bits are recorded before the six least significant bits.

d. Calibration

Three dummy characters are recorded after the record ID character, and one dummy character is recorded after the attenuator setting character. In addition, the frequency characters are recorded in reverse order.

e. CCIR Noise

The two characters representing the amplitude are interchanged.

SECTION V

MODE PROCESSOR

The mode processor provides the capability to separate four modes of propagation, sample the peak signal of each of these modes, and hold this peak until the next sample period. This function is performed for both mode loss and angle of arrival. The design of this unit was described in the previous report. Since minor changes are still being made to this equipment in the integration phase, complete installation and operating instructions will not be presented until the final report.

SECTION VI

ABSOLUTE TIME EQUIPMENT

To accurately determine the propagation loss for the individual modes of propagation being measured at any given time, the antenna gain for both transmit and receive must be known for each mode. The antenna gains for a particular mode are dependent on the elevation angle of takeoff and arrival. These angles are assumed equal and are determined from the Breit and Tuve theorem by use of the measured propagation time for the mode. To obtain the desired accuracy in the calculated propagation loss for low radiation angles and the antennas employed, the propagation time for each mode should be measured to our overall tolerance of $\pm 20\,\mu s$.

A number of measurement techniques were investigated to meet this requirement for the Expanded Little IDA program. A timing system employed the Loran-C hyperbolic navigation system was selected as the most suitable after considering such items as cost, accuracy, resettability, etc. This system makes use of the fact that the east-coast stations of Loran-C transmit their signals at times very accurately related to both one another and the absolute time kept by the United States Naval Observatory (coordinated UT-2 or UTC time). Furthermore, since the Loran-C signals are transmitted in the LF band (100 kHz to be exact), at least one of the east-coast stations can be received via groundwave propagation at all of the Expanded Little IDA field sites. One advantage of LF groundwave propagation is that the propagation time has very little variation as a function of time, and hence can be accurately determined. This delay can be added to the other known system delays to establish the absolute time (epoch) at each site. If each transmitted signal occurs at a known time with respect to the established epoch, the propagation time can be measured directly at the receive site if they also have the epoch. Descriptions of the use of Loran-C for such timing purposes may be found in References 3 and 4.

The ultimate timing objective would be to establish at each site an absolute time that is within $\pm 10\,\mu s$ of UTC. (References 5, 6, and 7 contain discussions of these terms; Reference 5 is particularly good.) This requirement can be relaxed somewhat since it is only necessary that the epochs established at the Expanded Little IDA sites be accurate to one another with this precision rather than to UTC time. This means a fixed constant offset can exist at all sites, provided that it is the same. It is anticipated that for simplicity a constant offset will probably be maintained at all sites.

The equipment provided to establish an accurate time at each site consists of the following: a Collins LR-201 Loran-C timing system, a Hewlett Packard 106AR quartz oscillator, a Granger Associates 540 clock programmer, a Hewlett Packard 526B time interval counter, an oscilloscope, a phase difference recorder, an R390A HF receiver, and sampling equipment. The time standard or clock consists basically of the quartz oscillator and the clock programmer. The other equipment is used for setting the clocks and for determining the actual transmission times of the Phantom and sounder signals. A block diagram showing the configuration of the absolute time equipment is provided in the lower third of Figure 2.

At each site, the clock is initially set to approximately UTC time using an HF skywave propagated timing signal such as provided by WWV. This signal is a series of pulses occurring on the second, with periodic voice announcements giving the time of day (Reference 7 contains a discussion of these timing signals). Because of the uncertainties in predicting the HF skywave propagation time of such a signal, the accuracy obtained using this technique for setting the clock is about one ms. Thus, the clock at each site is set with time of day information and to UTC rather coarsely when compared to the ultimate accuracy which is needed. Groundwave Loran-C transmissions are then used to set the clocks at each site to within $\pm 10\,\mu s$ of the desired UTC time. Since the time initially established at each site is dependent on calculated values of propagation time for each path, it is planned to have the U.S. Naval Observatory compare the time settings at each site as established using Loran-C with UTC time as maintained by the Observatory. A travelling clock service exists at the U.S. Naval Observatory to perform this function. An atomic clock that has been compared against the United States time standard is transported to the remote site. By this means, clocks at distant locations can be compared against international time standards. The technique of using portable clocks for this purpose is described in References 8 and 9.

At the transmitter sites, a comparison will be made between the start of the actual transmitted signals -- Phantom and sounder -- and the beginning of a 100-pps timing signal derived from the time standard whose occurrence has been related to UTC time. Any measurable time differences will be removed by suitably advancing or delaying the transmitted signal. To obtain long-term time stability, a phase-difference recorder will provide a graphic display of the difference between the Loran-C frequency and the site frequency standard. This will supply the information needed to correct for and to anticipate drifts in the field site frequency standards.

At the central receiver site, a comparison will be made between the time of arrival of each mode selected by the mode processor and the 100-pps timing signal which has been derived from the site time standard. This 100-pps signal has been related to UTC time the same as the transmitter site signal. Transmission time uncertainties of 10 ms, 20 ms, etc. will exist due to the 100-pps timing signal. This can easily be removed by determining the approximate HF skywave transmission time which can be calculated with an accuracy of about 1 ms for the distances involved.

SECTION VII

SOUNDERS

The specifications for the sounder network were described in Interim Report No. 1. The sounders to meet these specifications were produced by Granger Associates, Palo Alto, California. The order was composed of two new sounder transmitters for the two new remote sites, and updating of the equipment already in place at Stockbridge and Coco Solo. The design is an adaption of Granger's standard line. The most important changes are to cover the frequency range of 4 to 64 MHz and to incorporate the HP 106AR as the frequency standard, rather than the HP 103AR. This change permits time-keeping accurate to within 10 μs by use of the Loran-C timing system.

For design details, installation, alignment, and operating instructions, the reader is referred to the instruction books for this equipment.

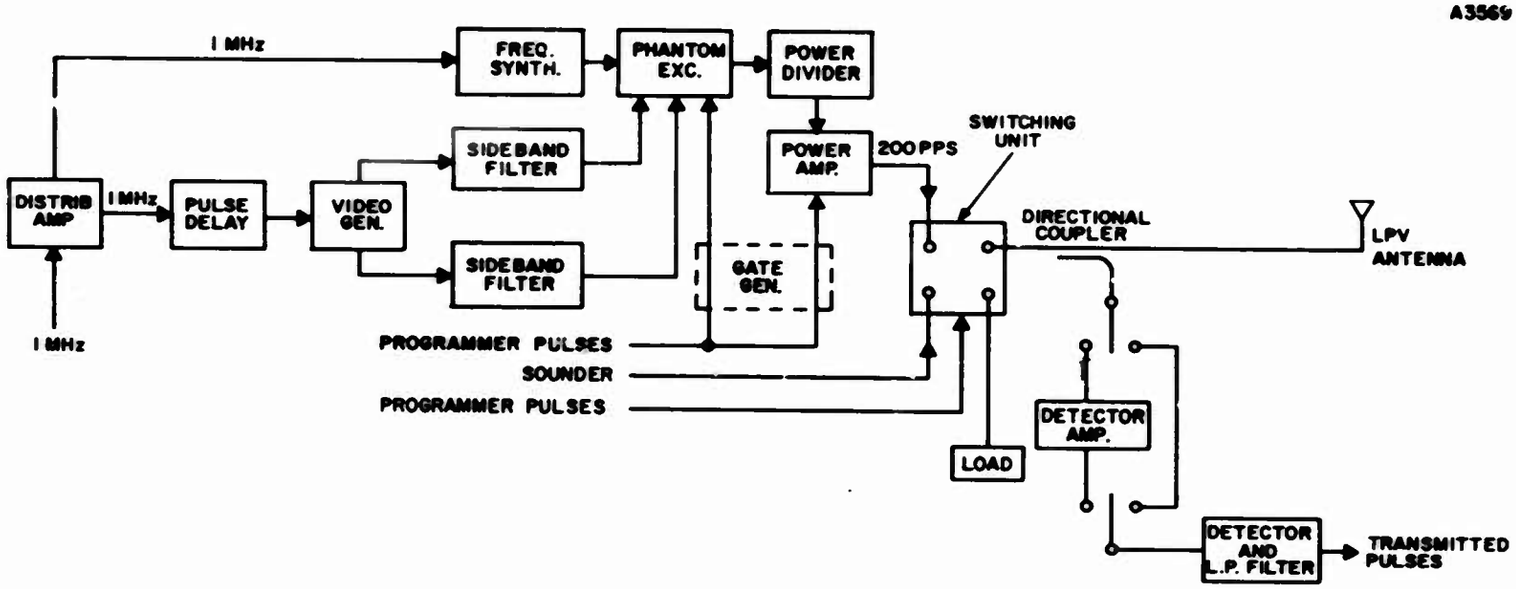


Figure 54. Phantom Transmitter

SECTION VIII

PHANTOM EQUIPMENT

1. INTRODUCTION

The basic concept and the overall block diagram of the Phantom system is adequately described in Interim Report No. 1. In addition, the receiver system is basically unchanged from the previous program. Hence, in this report, attention will be given only to the design of the transmitter chain for the two new remote sites.

2. TRANSMITTER DESIGN

The transmitter system is shown in block diagram form in Figure 54. A discussion of each of the components follows.

a. Distribution Amplifier

The distribution amplifier (shown in Figure 55) provides a means of distributing the frequency standard (1-MHz) signal to other units of the transmitter site. Four outputs are provided: sounder programmer (Z_o = 500Ω), frequency synthesizer (Z_o = 330Ω), pulse delay (Z_o = 1000Ω), and spare (Z_o = 500Ω). The unit consists of four common emitter amplifiers, each having approximately unity gain. The frequency standard signal is applied to the base of each amplifier. A supply voltage of 12 v dc is required and may be obtained from the 12-v dc supply in the Phantom video generator.

b. Pulse Delay Unit

(1) Function

This unit accepts a 1-MHz sine wave and generates a 100-kHz square wave. This square wave can be delayed up to 5.461 ms by setting in a desired delay with toggle switches on the front panel and depressing a DELAY switch.

(2) Detailed design

Two printed wire boards make up the pulse delay unit. Figure 56 shows how the boards and switches are wired together.

(a) Interface Board Assembly

This assembly (shown in Figure 57) performs the following functions.

1. Converts 12 v to 4.5 v -- a voltage divider is used to get the voltage down to 4.5 v and a transistor driver is used to provide the current

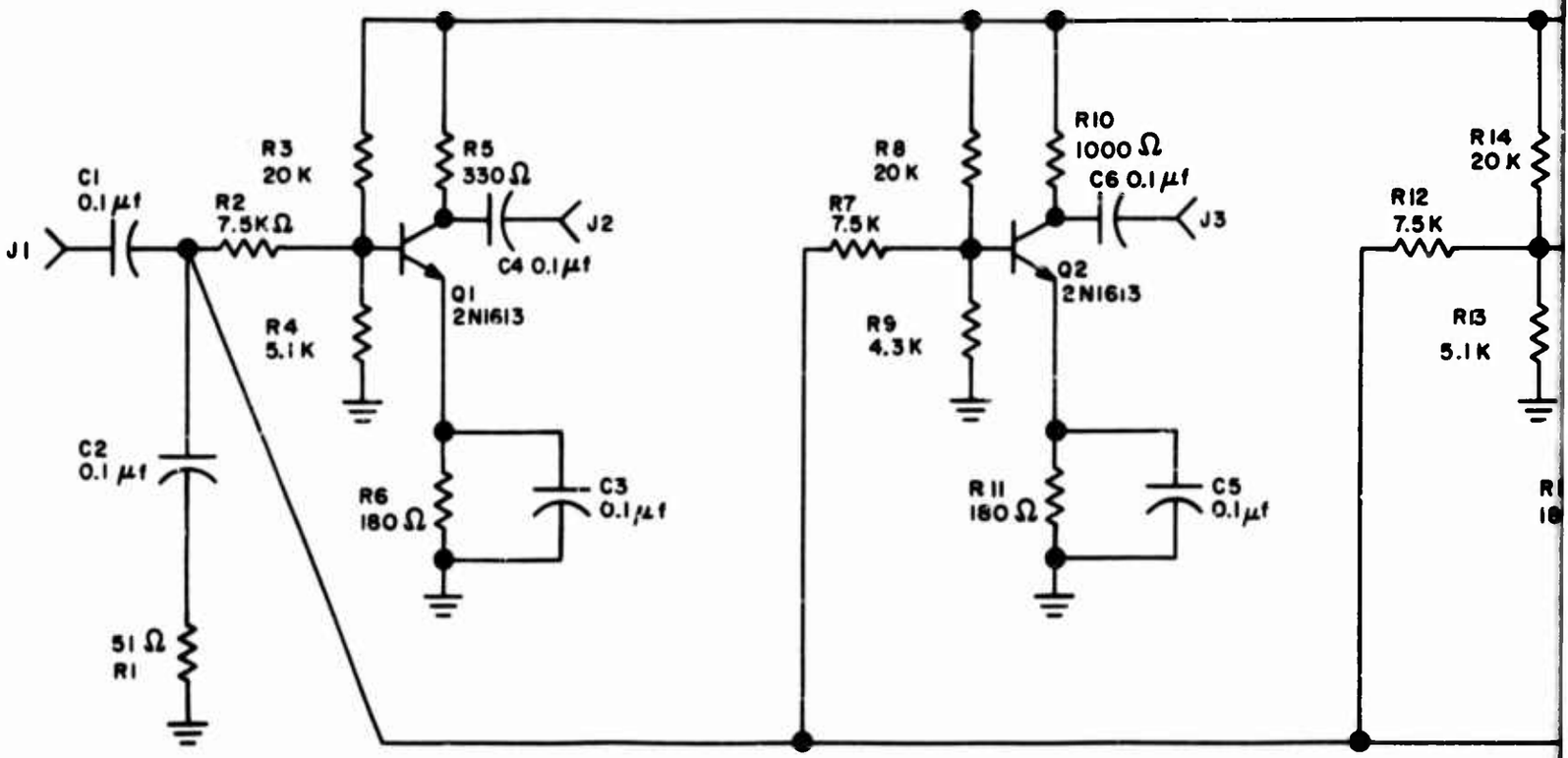
necessary to run the logic board assembly.

2. Sine-to-pulse converter -- this circuit accepts a 1-MHz, 0.5-v rms, sine wave and generates a 1-MHz clock pulse which is used by the logic board assembly; the circuit consists of a tuned amplifier stage and two current gain stages.

3. Pushbutton switch sensing circuits -- an integrated circuit flip-flop is used to take out the switch bounce; the flip-flop will be set and reset only once each time the switch is pushed. The flip-flop then drives a one-shot multivibrator which generates a reset pulse. The output of the multivibrator drives a second multivibrator which generates a set pulse.

(b) Logic Board Assembly

This board (shown in Figure 58) contains a gated divide by 10 counter consisting of flip-flops A22, A15, A6, and A7. The output of flip-flop A7 is a 100-kHz square wave. The 13-stage binary counter on the board determines the amount of time to delay the 100-kHz sine wave. The delay is accomplished by preventing the divide by 10 counter from counting the 1-MHz clock pulses. When the operator depresses the DELAY pushbutton a reset pulse is generated that puts all zeros in the 13-stage binary counter. The set pulse, which follows the reset pulse, will put ones in the even numbered stages of the binary counters as well as those odd number stages not selected from the control panel. (The odd number stages represent delays of 1, 4, 16, 64, 256, 1024, and 4096 μs.) The set pulse allows flip-flop A21 to be set which disables the divide by 10 counter and enables the 13-stage counter. When the 13-stage counter has all ones in it, the output of gate A12 will go up which will allow control flip-flop A21 to be reset. This stops the 13-stage counter and allows the divide by 10 counter to run, thus restoring the 100-kHz square wave.



NOTE: 1. ALL RESISTORS 1/4 W
2. ALL CAPACITORS 50 VDC

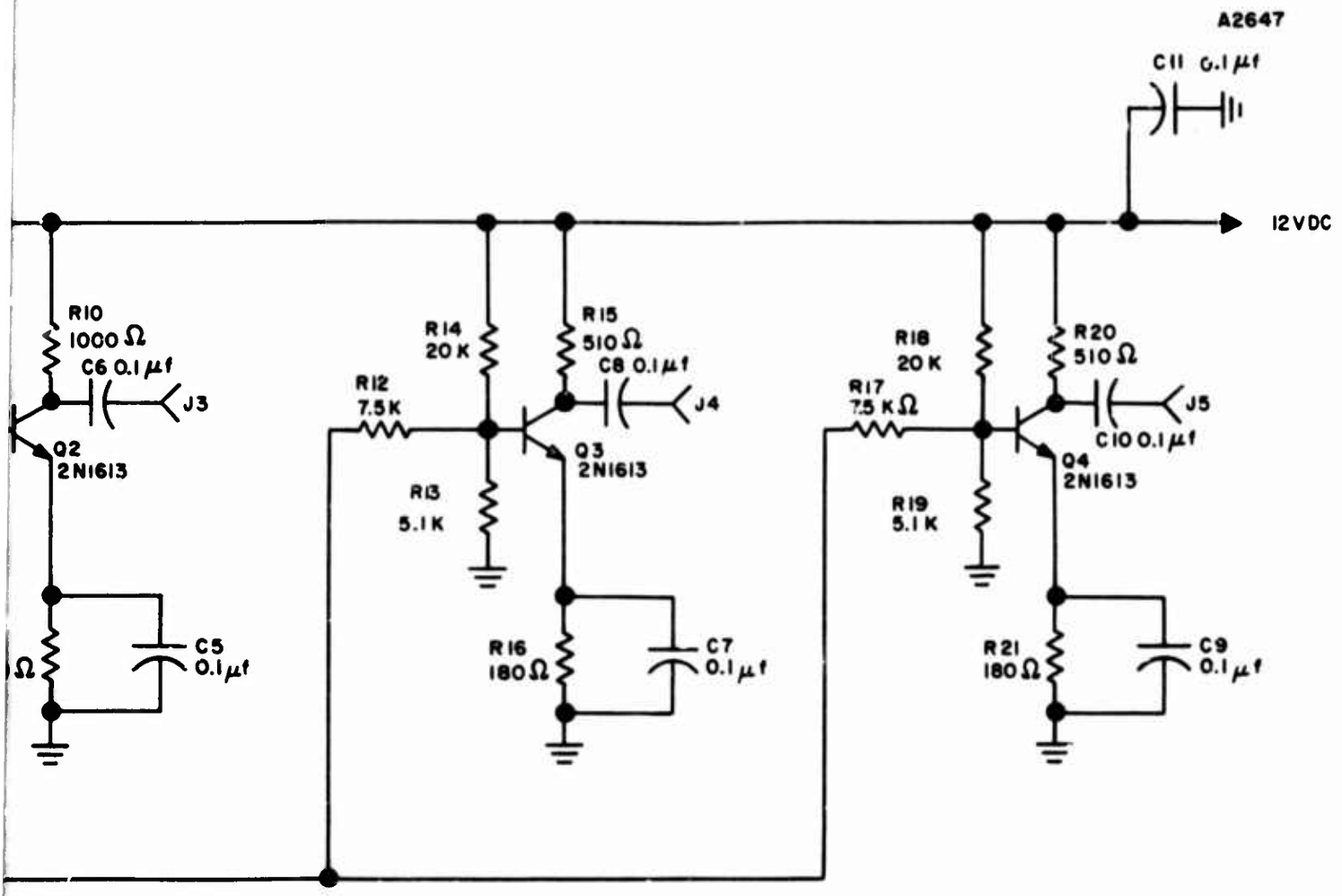


Figure 5?. Distribution Amplifier

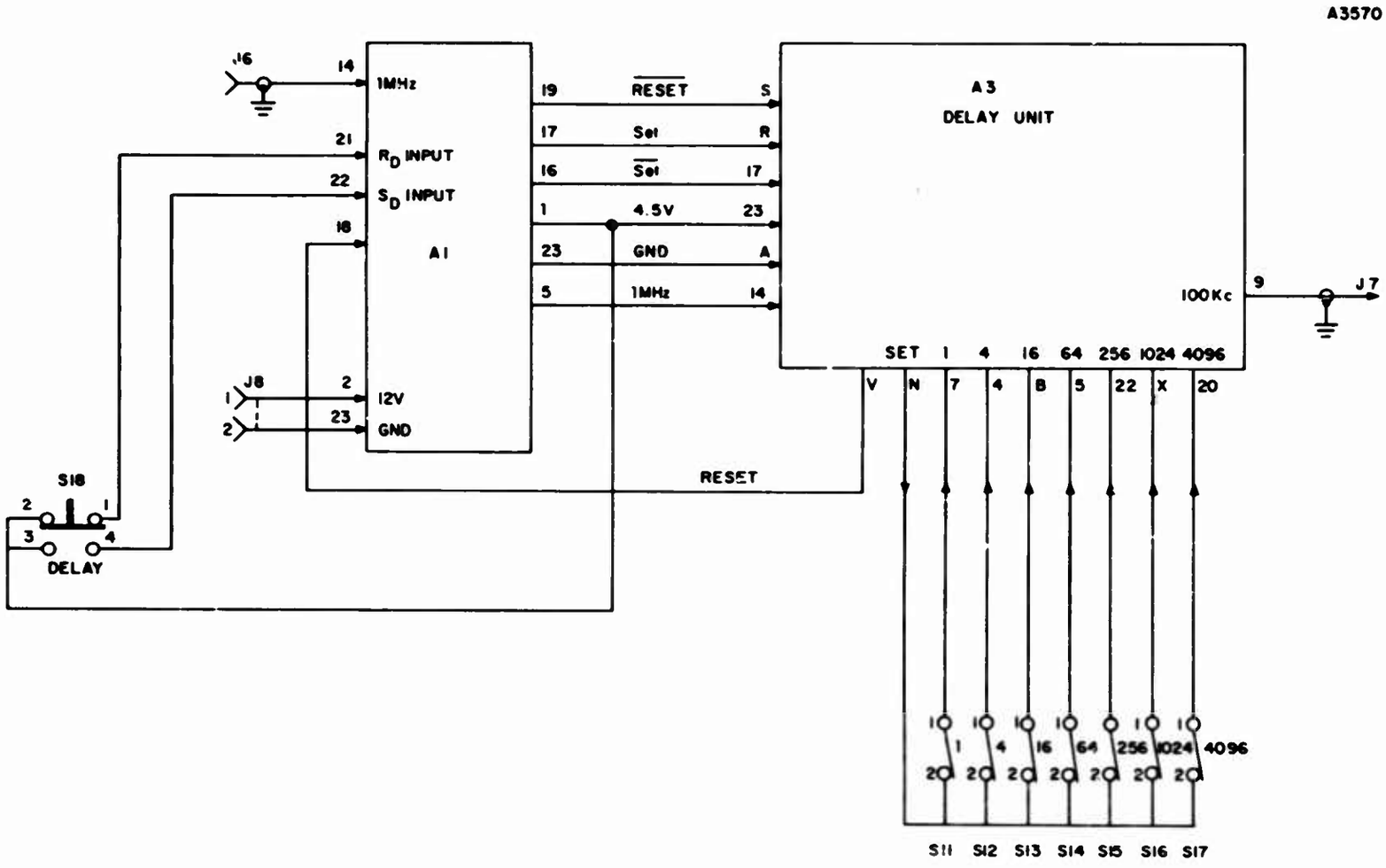


Figure 56. Pulse Delay Unit Interconnection Diagram

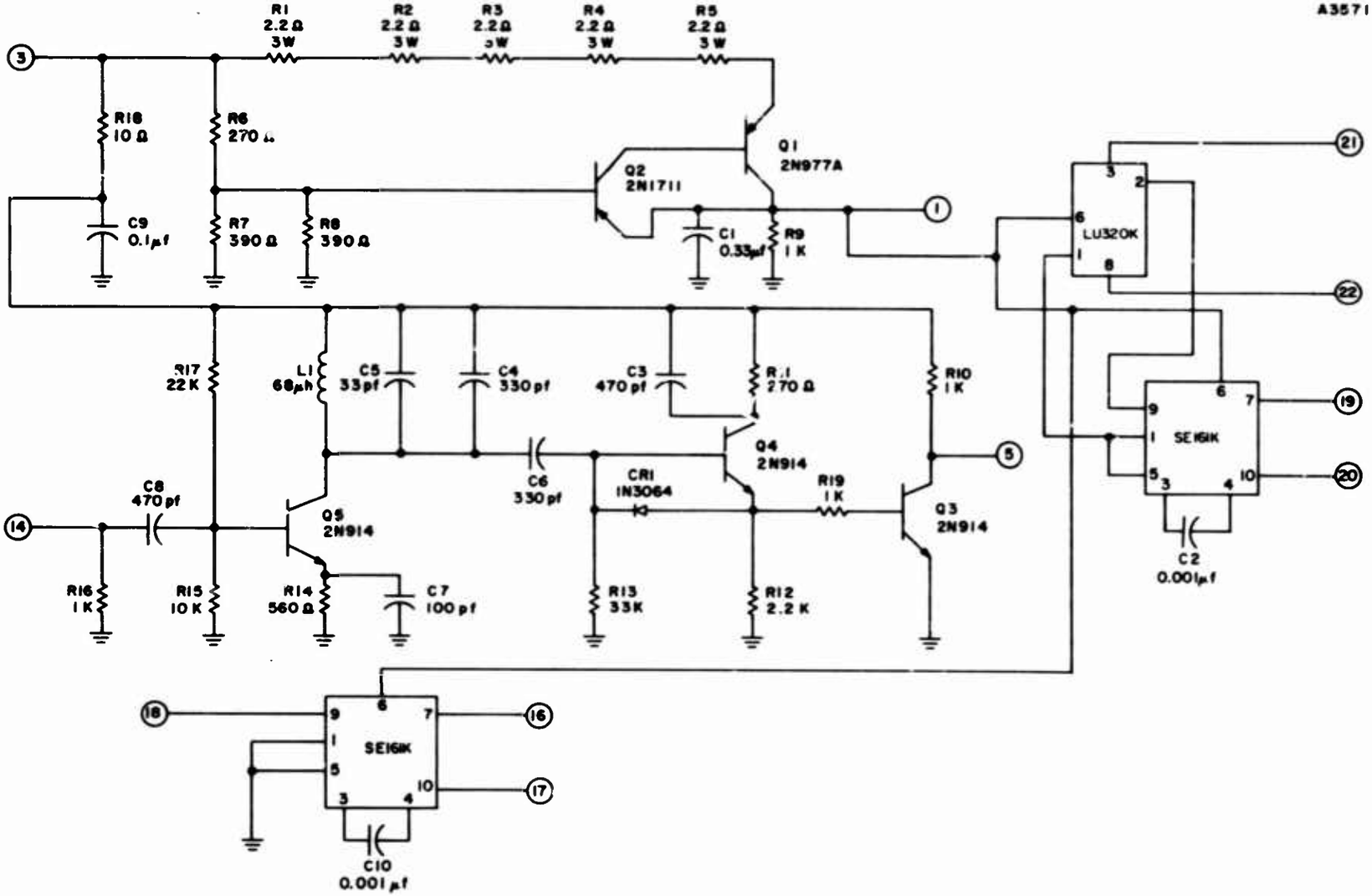
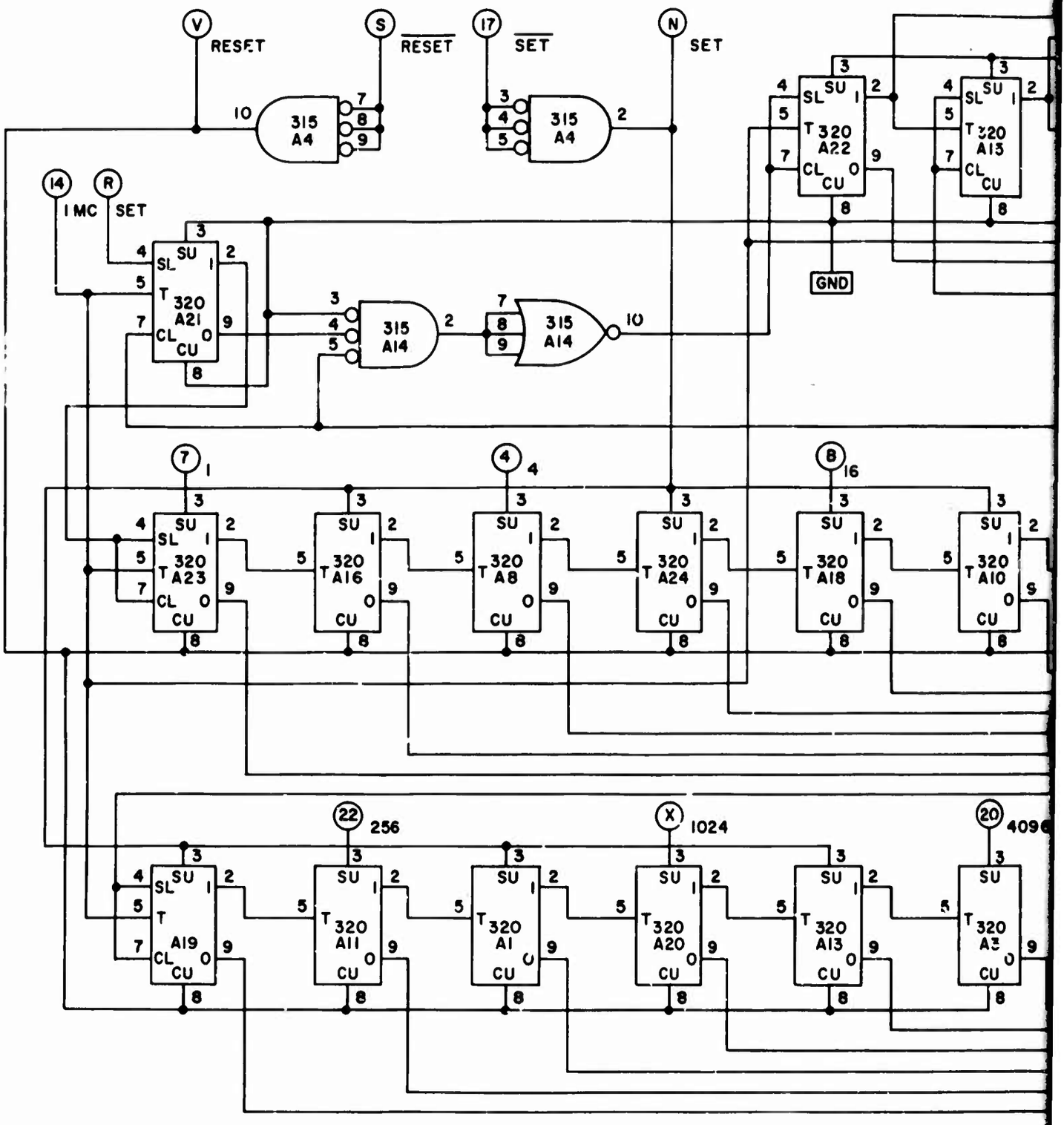


Figure 57. Interface Board Assembly


V
RESET
S
RESET
17
SET
N
SET
315 A4
315 A4
14
1 MC
R
SET
320 A21
315 A14
315 A14
GND
320 A22
320 A13
7
1
4
4
8
16
320 A23
320 A16
320 A8
320 A24
320 A18
320 A10
22
256
X
1024
20
4096
320 A19
320 A11
320 A1
320 A20
320 A13
320 A3

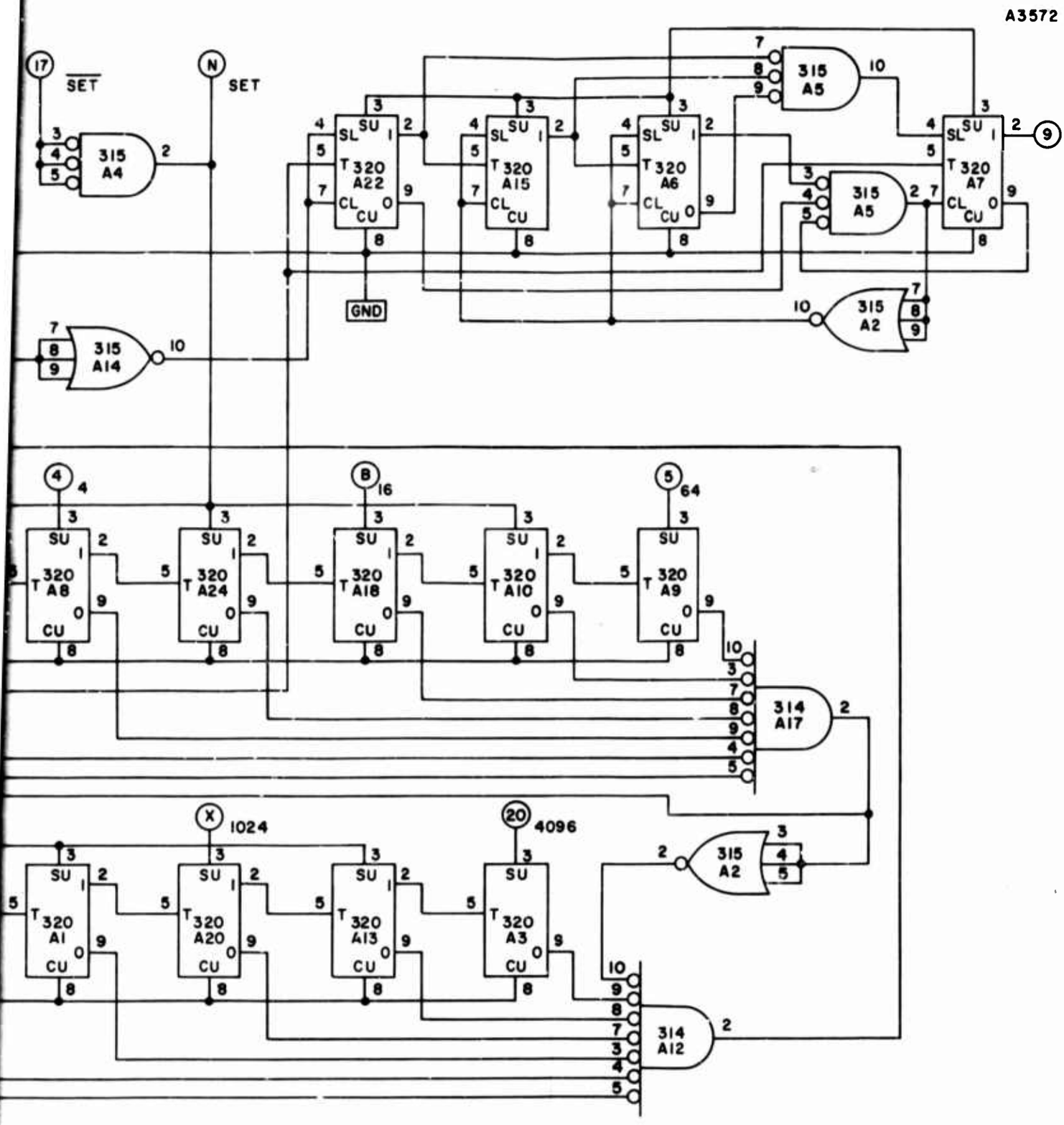


Figure 58. Logic Board Assembly

2

c. Phantom Video Generator

The Phantom video generator (shown in Figure 59) produces a binary coded video signal which is synchronized with the frequency standard. The 100 kHz derived from the frequency standard is applied to the video generator through J1 and R1. R1 is adjusted for a signal swing from -11 to -3 v at the collector of Q1. At this point the signal is supplied to the digital processing section which consists of digital circuit modules. In this section, the CW signal is converted to a pulse signal and the codes are formed. The outputs of the video generator are J3 and J4 which are identical in time but opposite in state polarity. R12 and R13 have been added to insure proper loading of the output gates while working into a 50-ohm load. A control input, J2, is provided at the rear of the unit to disable the video generator during the tuning of the Phantom exciter. The two output gates are enabled when ground is applied through the exciter mode switch in the MOD position.

The mode switch on the front panel provides four modes of operation: $\frac{13}{13} - \frac{13}{13}$, 13, $\frac{13}{13}$, and $13 - \frac{13}{13}$. All codes are of the form shown in Figure 60.

A3573

Figure 60. Optimum Barker Code

The two states correspond to 0° or 180° phase coding at the output of the Phantom exciter. Mode 2 (13) provides a 13-bit code of 130-μs pulses with the code occurring at a repetition rate of 100 pps. The total code time is 1.69 ms with a dead time of 8.31 ms. In mode 3($\frac{13}{13}$), each 130-μs pulse is further coded with thirteen 10-μs pulses. The polarity of this code depends on the polarity of the 130-μs pulse. The repetition rate of the resultant 169-bit code is 100 pps. Mode 1 ($\frac{13}{13} - \frac{13}{13}$) is the same as mode 3 only with a PRF of 200 pps. The $13 - \frac{13}{13}$ mode (4) provides one code of 13 type code (code time 1.69 ms) while the next code is of the $\frac{13}{13}$ (code time 1.69 ms) type. Alternation of this coding is continuous at a repetition rate of 200 pps.

The outputs of the video generator are applied to the Phantom exciter through a set of sideband filters. Test jacks are provided on the front panel for scope sync or monitoring purposes. Also, meters are provided for monitoring the current drain on the plus and minus power supplies.

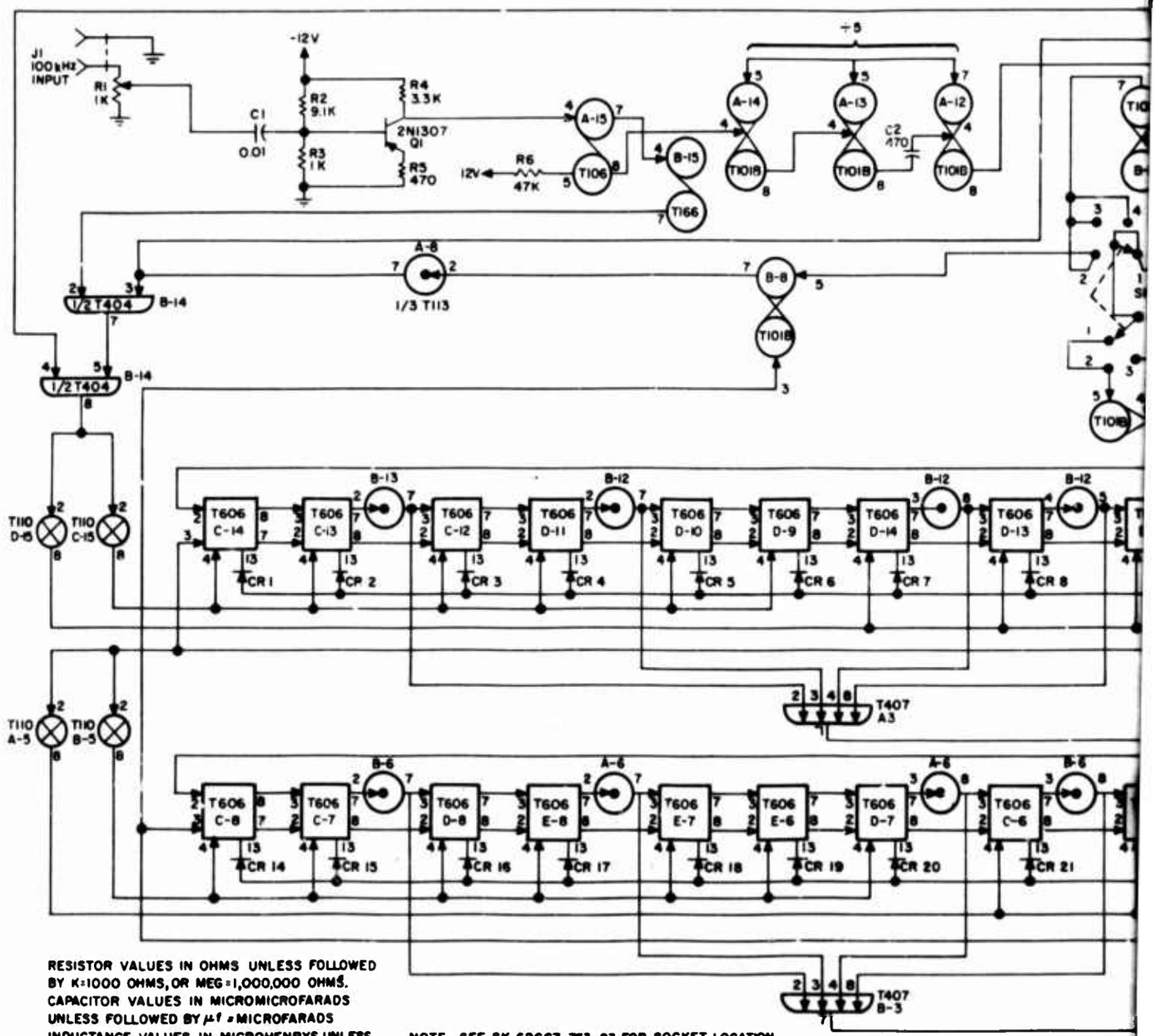
d. Frequency Synthesizer

The frequency synthesizer is a Manson MHS-400 precision frequency generator which provides frequencies in the 2- to 34-MHz range. The 1-MHz frequency from the distribution amplifier unit is the primary synthesizer reference. The output level is 0.1 to 2.5 v rms into 50 ohms. The signal from this unit is used to drive the RF section of the Phantom exciter.

e. Phantom Exciter

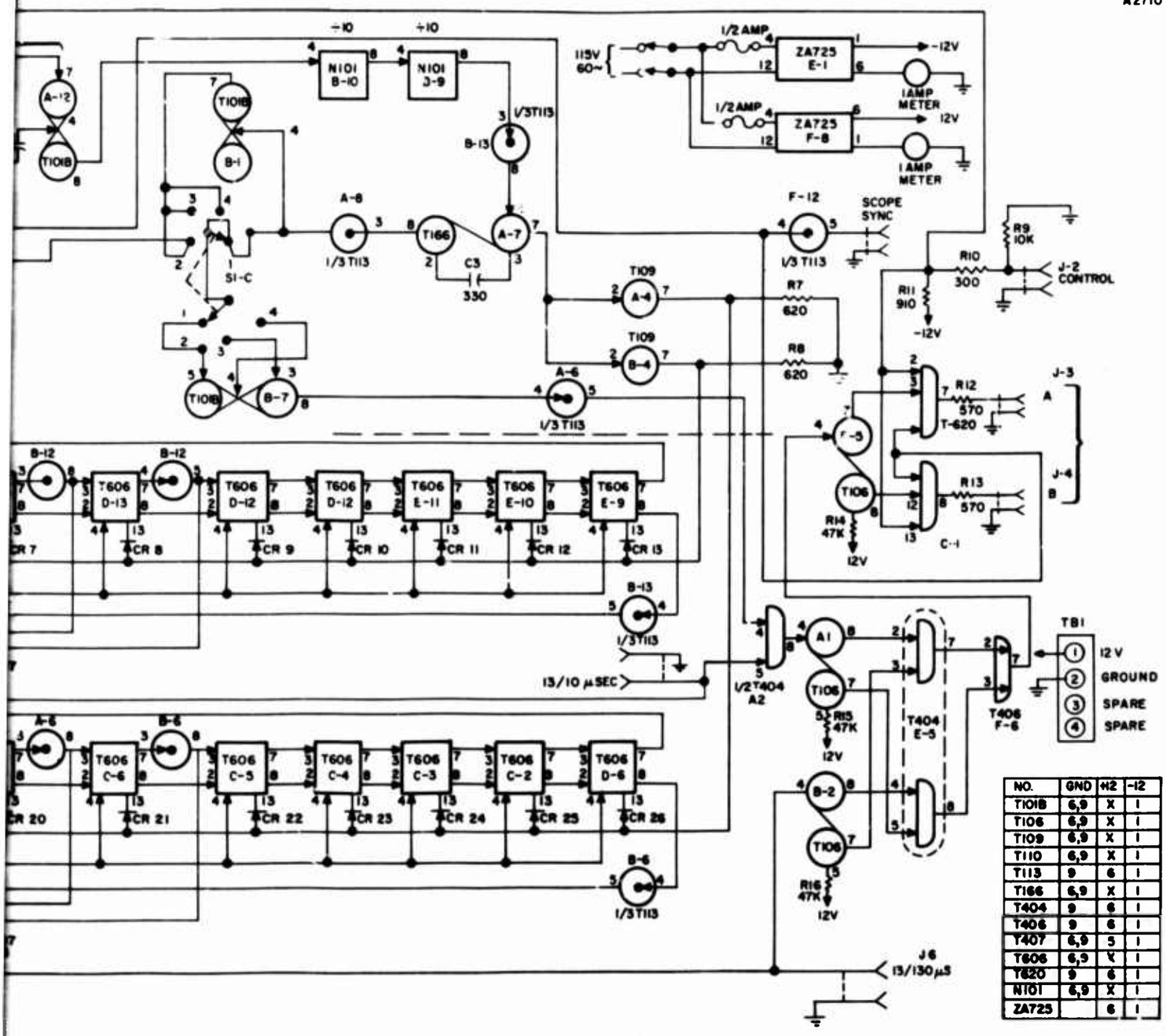
The Phantom exciter (shown in Figure 61) is a pulse modulator, capable of amplitude and phase modulation (0° or 180° phase) over an RF range of 5 to 30 MHz. The peak power available is approximately 20 W. MOD 1 and MOD 2 inputs (J3 and J4) are a binary code generated in the Phantom video generator. The RF input (J1) is the RF carrier generated by the frequency synthesizer. The modulation section, which consists of two video channels -- V7A/V8/V9 and V7B/V6/V5 -- is a class A amplifier that drives the screen grids of modulator tubes V3 and V4. The signal appearing on the screen grid may be adjusted to provide correct peak-to-peak voltage swing and dc voltage level by adjustments R3, R4 and R28, R29 respectively. The RF section, consisting of V1 and V2, is a tuned RF amplifier with 0° and 180° phase outputs. This section is tunable from 5 to 30 MHz in three bands: 5 to 9, 9 to 16, and 16 to 30 MHz. One phase is applied to the control grid of V3 while the other is applied to the control grid of V4. A meter is provided on the front panel of the exciter to monitor grid current. The two modulator tubes are 6146's and share a common load. The plate load is a pi-network that is tuned by C5 and L10, which are mechanically connected, and C22. The plate voltage is variable from 0 to 750 v dc with 400 v dc being the recommended value. During normal operation (mode switch in MOD position), the dc voltage levels on the screen grids of V3 and V4 are approximately equal so that during the dead time between codes (3.31 or 6.62 ms) RF cancellation occurs in the common plate load. During code time, the video signals appear on the screen grids and control conduction of the tubes. Since the code signals are of opposite polarity, one tube will conduct more than the other allowing only one RF phase to appear at the output (J8 or J9) representing a particular state of the code. The amplitude of the output signal is proportional to the amplitude of the modulating signal.

In order to tune the output circuit of the exciter, it is necessary to adjust the dc levels of the modulation signal so that one phase is continuously present at the output; no modulation is desired. The mode switch (S2) is provided for this purpose. S2-A provides a means of controlling the output of the Phantom video generator. In the MOD position, ground is present at J2, enabling the video generator. In the CW position, J2 is open and there is



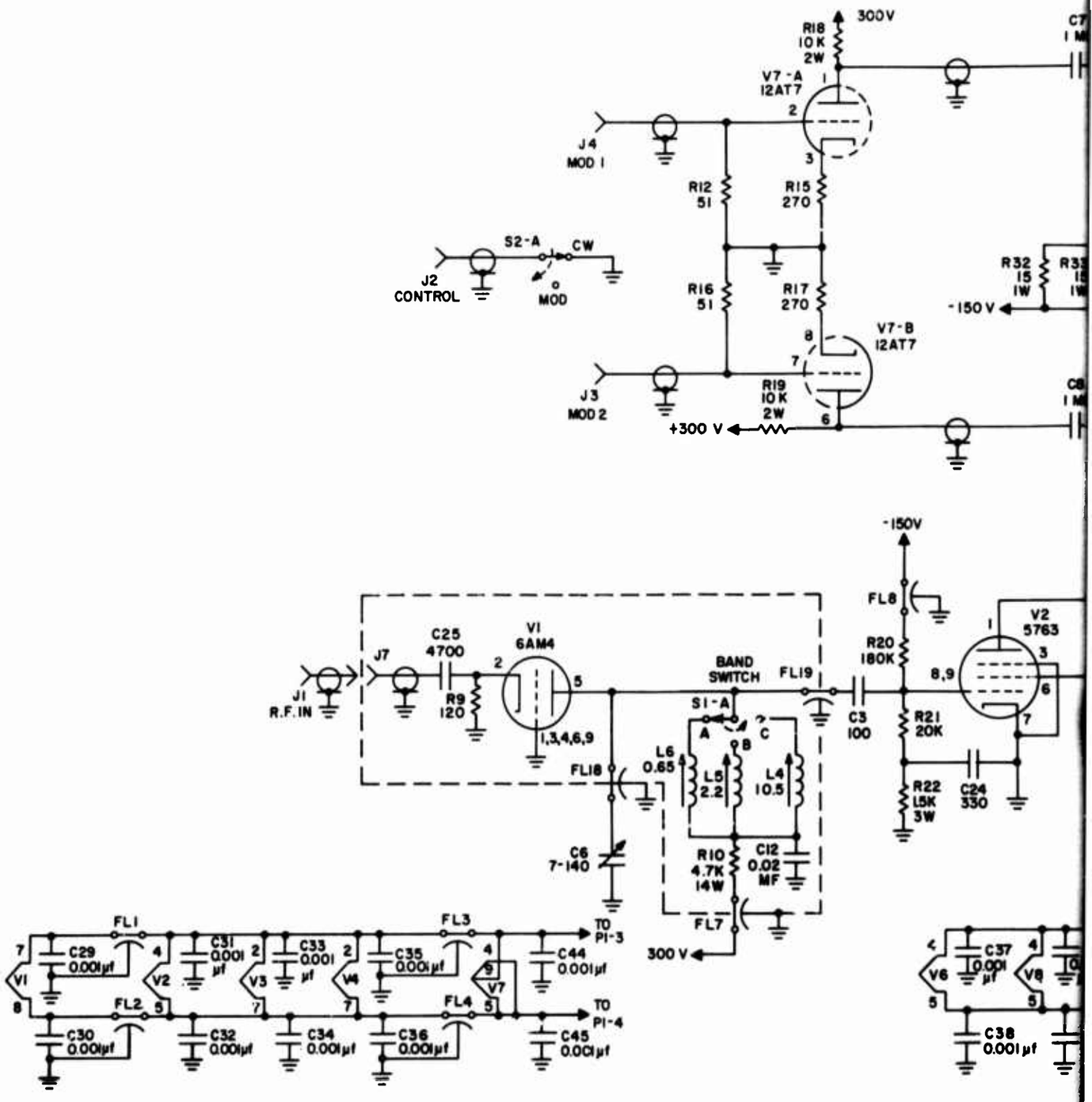
RESISTOR VALUES IN OHMS UNLESS FOLLOWED BY K=1000 OHMS, OR MEG=1,000,000 OHMS.
CAPACITOR VALUES IN MICROMICROFARADS UNLESS FOLLOWED BY μf = MICROFARADS
INDUCTANCE VALUES IN MICROHENRYS UNLESS FOLLOWED BY MH=MILLIHENRYS OR H=HENRYS.

NOTE SEE SK-62667-753-93 FOR SOCKET LOCATION
ALL DIODES ARE 1N198
SWITCH SHOWN IN POSITION 1



NO.	GND	+12	-12
T101B	6,9	X	1
T106	6,9	X	1
T109	6,9	X	1
T110	6,9	X	1
T113	9	6	1
T166	6,9	X	1
T404	9	6	1
T406	9	6	1
T407	6,9	5	1
T606	6,9	X	1
T620	9	6	1
N101	6,9	X	1
ZA725		6	1

Figure 59. Phantom Video Generator


300V
R18 10K 2W
V7-A 12AT7
J4 MOD 1
R12 51
R15 270
S2-A
CW
MOD
J2 CONTROL
R16 51
R17 270
V7-B 12AT7
J3 MOD 2
R19 10K 2W
+300 V
R32 15 1W
-150 V
-150V
FL8
V2 5763
R20 180K
8,9
R21 20K
R22 15K 3W
C24 330
J7
C25 4700
V1 6AM4
J1 R.F. IN
R9 120
1,3,4,6,9
BAND SWITCH
FL19
S1-A
A
B
C
C3 100
FL18
L6 0.65
L5 2.2
L4 10.5
C6 7-140
R10 4.7K 14W
C12 0.02 MF
FL7
300 V
FL1
FL2
FL3
FL4
C29 0.001µf
C30 0.001µf
C31 0.001 µf
C32 0.001µf
C33 0.001 µf
C34 0.001µf
C35 0.001µf
C36 0.001µf
C44 0.001µf
C45 0.01µf
TO PI-3
TO PI-4
V1
V2
V3
V4
V5
V6
V8
C37 0.001 µf
C38 0.001µf

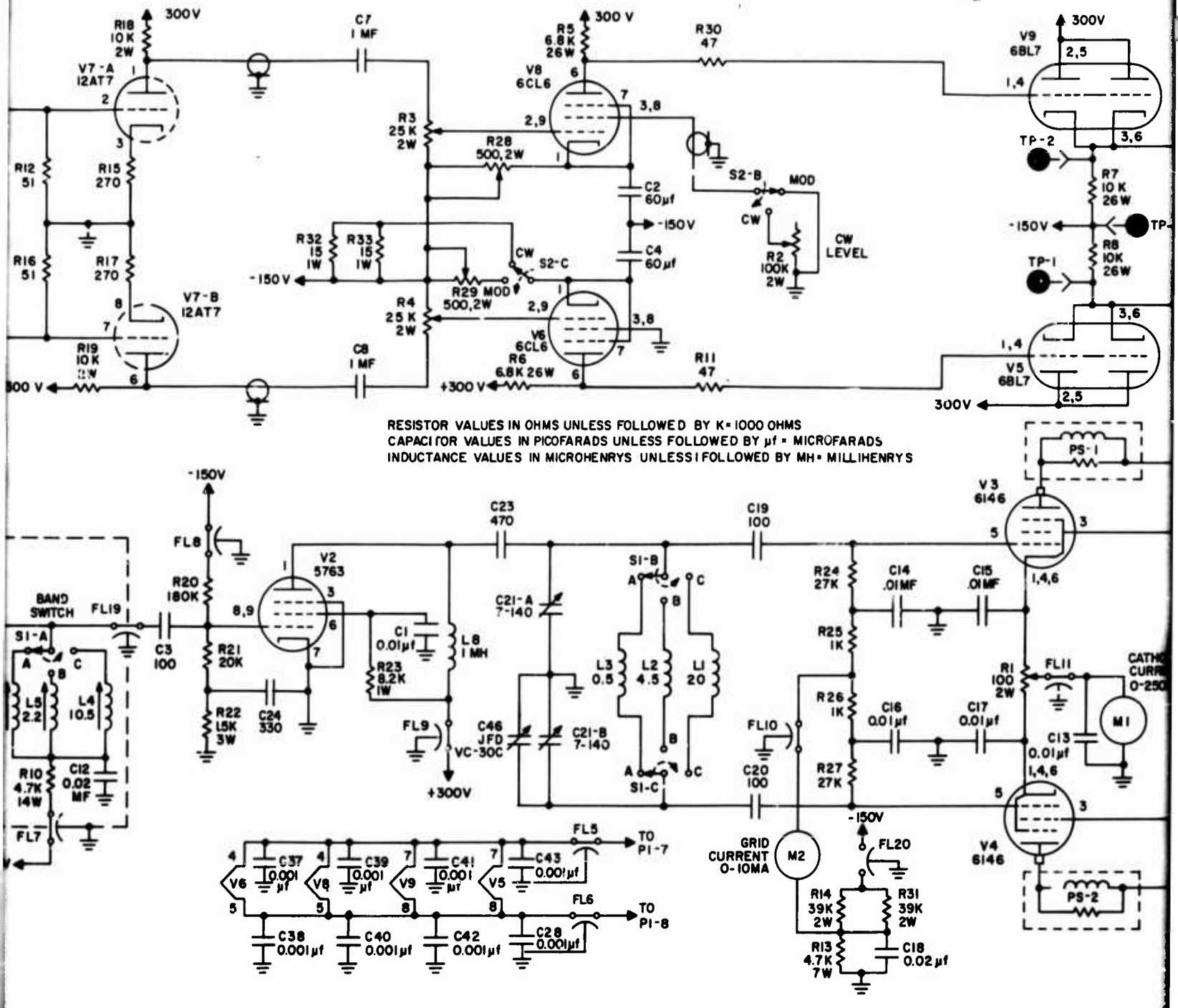
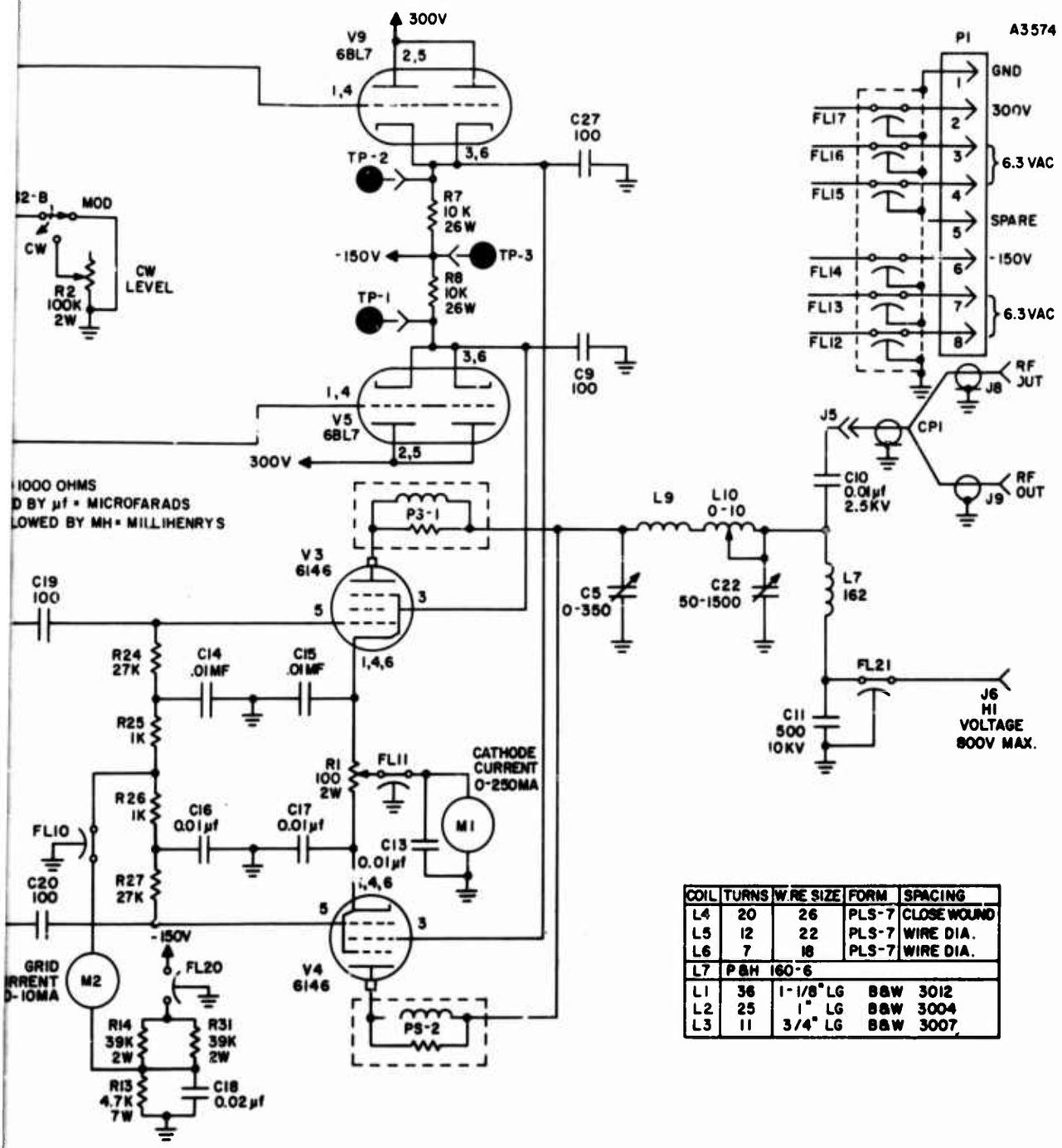


Figure 61. Phantom Exciter



COIL	TURNS	W.RE SIZE	FORM	SPACING
L4	20	26	PLS-7	CLOSE WOUND
L5	12	22	PLS-7	WIRE DIA.
L6	7	18	PLS-7	WIRE DIA.
L7	P&H 160-6			
L1	36	1-1/8" LG	B&W	3012
L2	25	1" LG	B&W	3004
L3	11	3/4" LG	B&W	3007

3

no output from the video generator and no modulation at the output of the exciter. S2-C provides a means of insuring that V3 has a negative voltage on the screen grid during CW operation. This reduces the conduction of V3 and consequently its associated RF signal. S2-B provides a means of adjusting the conduction of V4 during CW operation. The phase associated with V4 is the phase seen at the output.

For optimum operation of the exciter, it has been found that there are definite voltage adjustments necessary in the modulation section. With the mode switch in MOD and J2, J3 open (no video inputs), R28 and R29 should be adjusted for 20 v dc at TP-1 and TP-2. Then, with J2 and J3 connected normally, R3 and R4 should be adjusted to provide 100 v peak-to-peak swing at TP-1 and TP-2.

To tune the exciter, it is necessary to set the sounder programmer for continuous Phantom operation. A tuning procedure for the Phantom exciter is given below.

1. Adjust the high voltage power supply for 200 v.
2. Place mode switch in CW position.
3. Adjust CW level for approximately 75 ma.
4. Turn band switch to the range within which the new frequency lies.
5. Tune the grid drive through range, stopping when maximum grid drive is reached as indicated on GRID ma meter. Reduce RF level on frequency synthesizer unit if meter attempts to go over 4 ma. After tuning for peak, adjust drive to 3 ma on GRID ma meter.
6. Turn ANTENNA COUPLING to minimum.
7. Tune PLATE TUNING for a dip in cathode current (CATHODE ma meter). Caution must be used to tune on the lowest frequency dip when operating at frequencies below 16 MHz due to harmonics. This can be avoided by starting PLATE TUNING at 0 dial calibration and then tuning to the first dip. A tuning chart may also be used.
8. Advance ANTENNA COUPLING toward the maximum position while monitoring the RF output (J8) with a high impedance oscilloscope. Adjust for maximum signal.
9. Readjust PLATE TUNING and ANTENNA COUPLING for maximum signal.
10. Set mode switch to MOD and adjust high-voltage supply to desired voltage.
11. Observe RF output. If RF is present during dead time between codes, adjust R28 for minimum. Adjust balance control for equal pulse amplitudes. If this cannot be accomplished, set balance control to midposition and adjust R3 for equal amplitudes.

f. Power Amplifier

This unit is a Gates HFL-3000 linear amplifier. It is a manually tuned amplifier capable of raising the amplitude of a 2- to 30-MHz, 100-mw signal to a level of 3-kW peak envelope power.

The bandwidth specified by the vendor is 16 kHz minimum; however, on one unit, the measured BW is 130 kHz minimum which is greater than the required minimum (100 kHz).

The input impedance is 50 ohms and the driving source is the Phantom exciter through a 15-dB power divider. Approximately 250 mW of RF is available from the power divider. A variable 1- to 10-dB attentuator has been provided to reduce the input to 100 mW.

In order to insure that the Phantom transmitter and sounder transmitter are not transmitting at the same time, both are controlled by the gate generator circuit located in the composite assembly (Figure 62). When the LOCAL-REMOTE switch at the power amplifier is in the REMOTE position, the PLATE VOLTAGE switch is bypassed and control of the high voltage power supply is assumed by the gate generator circuit. This is accomplished by connecting a set of gate generator relay contacts to terminal board 6TB5, terminals 3 and 4 of the power amplifier.

g. Composite Assembly

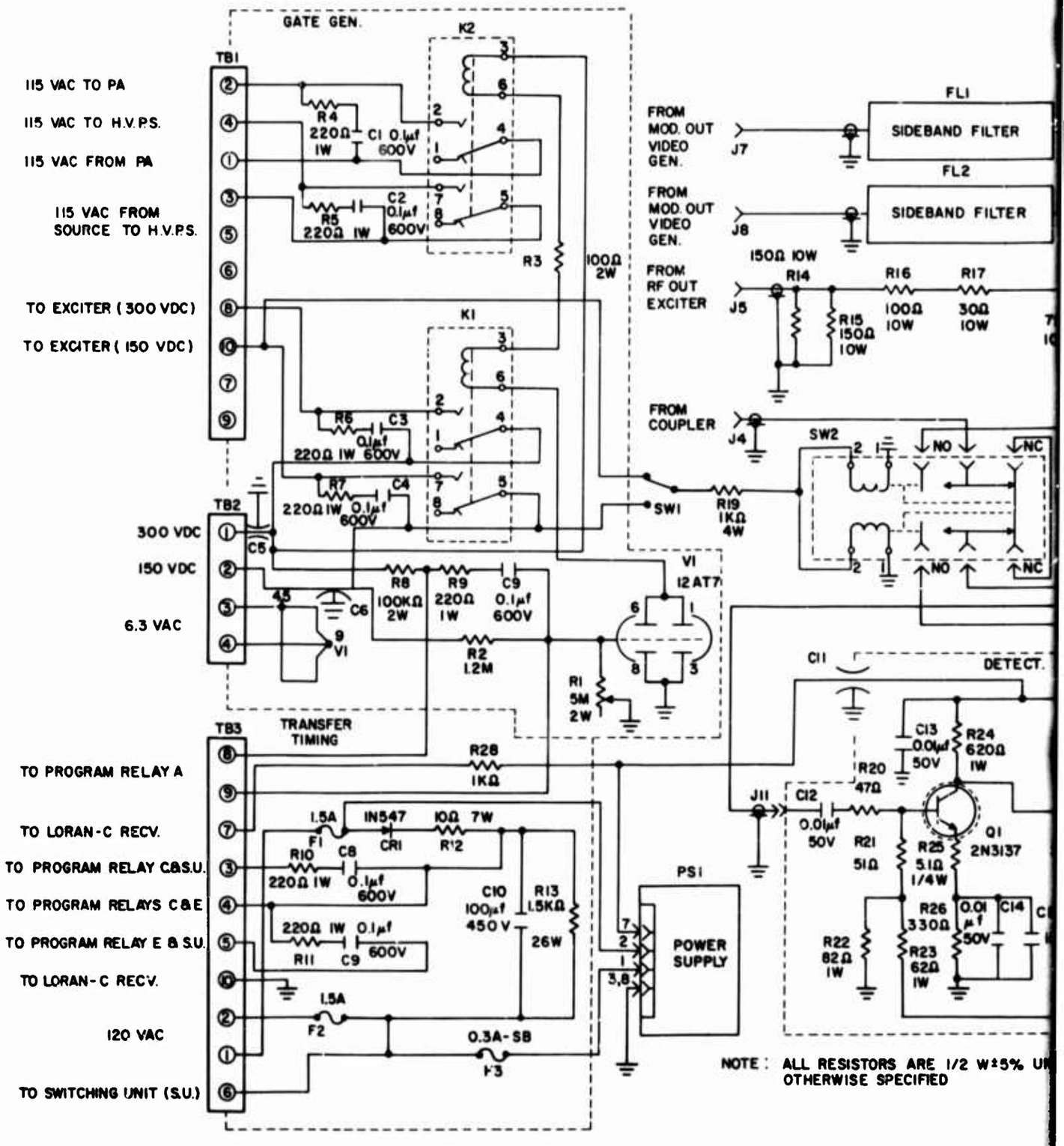
Located in this unit (shown in Figure 62) are several circuits necessary for Phantom operation.

(1) Gate Generator

The gate generator circuit provides a means of enabling the Phantom transmitter by controlling the RF exciter and power amplifier high voltages. The circuit is a vacuum tube switch (V1), turned on by the programmer, in which plate current operates relays K1 and K2. BIAS control R1, located on the back panel of the chassis, is adjusted for optimum relay action. The contacts of K1 control the RF exciter 300-v dc and -150-v dc power supplies. The contacts of K2 control the 115-v ac source for the RF exciter high-voltage power supply and the 115-v ac source for the power amplifier unit high-voltage power supply. The gate generator circuit is actuated by program relay A located in the sounder programmer (terminal board 9TB201, terminals 3 and 4).

(2) Transfer Timing

The transfer timing circuit is a dc power supply used to drive the switching unit. It furnishes 100 v dc at approximately 700 ma when the switch is being actuated. Control of the switching unit is provided by program relays C and E in the sounder pro-


GATE GEN.
K2
TB1
115 VAC TO PA
115 VAC TO H.V.P.S.
115 VAC FROM PA
115 VAC FROM SOURCE TO H.V.P.S.
TO EXCITER (300 VDC)
TO EXCITER (150 VDC)
R4 220Ω 1W
C1 0.1μf 600V
C2 0.1μf 600V
R5 220Ω 1W
R3 100Ω 2W
K1
R6 C3 0.1μf 220Ω 1W 600V
R7 C4 220Ω 1W 0.1μf 600V
TB2
300 VDC
150 VDC
6.3 VAC
C5
C6
R8 100KΩ 2W
R9 220Ω 1W
C9 0.1μf 600V
R2 1.2M
V1
12AT7
R1 5M 2W
SW1
R19 1KΩ 4W
FROM MOD. OUT VIDEO GEN.
J7
FL1
SIDEBAND FILTER
FROM MOD. OUT VIDEO GEN.
J8
FL2
SIDEBAND FILTER
150Ω 10W
FROM RF OUT EXCITER
J5
R14
R15 150Ω 10W
R16 100Ω 10W
R17 30Ω 10W
FROM COUPLER
J4
SW2
NO
NC
TB3
TRANSFER TIMING
TO PROGRAM RELAY A
TO LORAN-C RECV.
TO PROGRAM RELAY C&S.U.
TO PROGRAM RELAYS C&E
TO PROGRAM RELAY E & S.U.
TO LORAN-C RECV.
120 VAC
TO SWITCHING UNIT (S.U.)
R28 1KΩ
1.5A F1
IN547 CR1
10Ω 7W R12
R10 220Ω 1W
C8 0.1μf 600V
R11 220Ω 1W
C9 0.1μf 600V
C10 100μf 450V
R13 1.5KΩ 26W
1.5A F2
0.3A-SB F3
PS1
POWER SUPPLY
C11
DETECT.
J11
C12 0.01μf 50V
R20 47Ω
C13 0.01μf 50V
R24 620Ω 1W
Q1 2N3137
R21 51Ω
R25 5.1Ω 1/4W
R26 330Ω
R22 82Ω 1W
R23 62Ω 1W
0.01 μf 50V
C14
NOTE: ALL RESISTORS ARE 1/2 W ±5% UN
OTHERWISE SPECIFIED

1

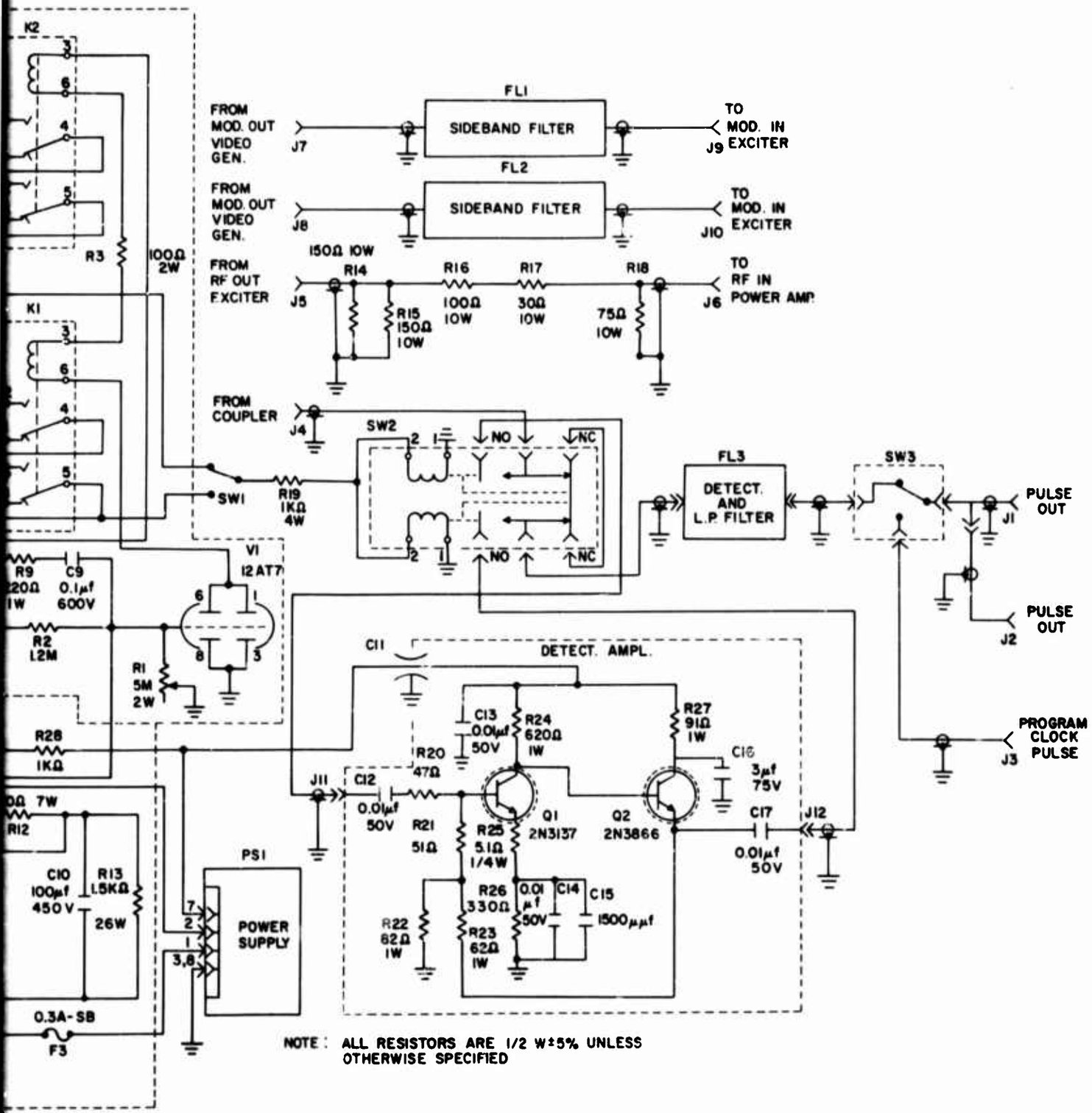


Figure 62. Composite Assembly

grammer. Figure 63 is a circuit diagram showing the transferring timing circuit and switching unit connections. Components C8, C9, R10, and R11 are provided for suppression at the relay contacts.

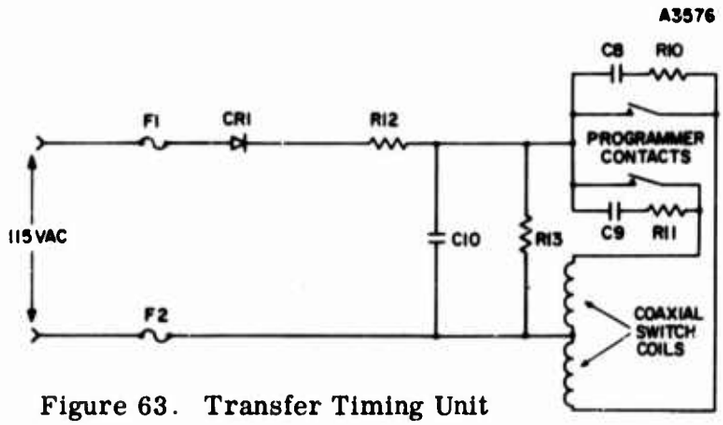


Figure 63. Transfer Timing Unit

(3) Detector Circuit

The detector circuit provides a sample of the RF output of the transmitter site in the Phantom mode or sounder mode. The circuit is composed of a Telonic RF detector (Type XD-8A), detector amplifier, and DPDT coaxial switch. The RF detector is linear over the required range (5 to 30 MHz) and provides a positive polarity dc output voltage in proportion to the rms input voltage. The detector amplifier is necessary to compensate for the difference in peak power between the Phantom (3-kW peak) and the sounder (30-kW peak). This represents a power ratio of 10/1 or 10 dB. When the sounder is transmitting, the coaxial switch actuating coils are not energized and the detector amplifier is bypassed. When the Phantom is transmitting, the coaxial switch coils are energized and the detector amplifier is in the circuit. The detector amplifier is a wide-band RF amplifier (5 to 30 MHz) which furnishes approximately 10 dB gain. It requires a 30-v dc supply voltage which is provided by PS1 (Acopian Model 30A4A). The input and output impedances of the amplifier and detector are 50 ohms The output of the RF detector is fed to the counter input switch (SW3), which selects the input to the time interval counter. In the CLOCK position, the input to the counter is a 100-pps clock pulse from the sounder programmer. The XMTR position provides an input from the detector circuit. The input to the counter may be monitored on the front panel of the composite assembly at the PULSE OUT jack (J2).

(4) Power Divider

The power divider circuit is between the Phantom exciter and the power amplifier. The power divider is a symmetrical pi-attenuator with input and output impedances of 50 ohms and furnishes 15 dB attenuation to the Phantom RF signal. This represents a power step-down ratio of 31.6/1 and provides approximately 250 mW to drive the power amplifier.

The power divider is composed of low inductance resistors R14-R18 in the composite assembly.

(5) Sideband Filters

In order to suppress sidebands due to pulse modulation at the output of the Phantom RF exciter, two low-pass filters are located between the video generator and the exciter. These filters have a 3-dB cutoff frequency of approximately 70 kHz and insertion loss less than 10 dB. The attenuation characteristic of a typical filter is shown in Figure 64. The input and output impedance is 50 ohms. These filters are found in the composite assembly (Figure 62) and are accessible by input jacks J7, J8 and output jacks J9, J10, respectively.

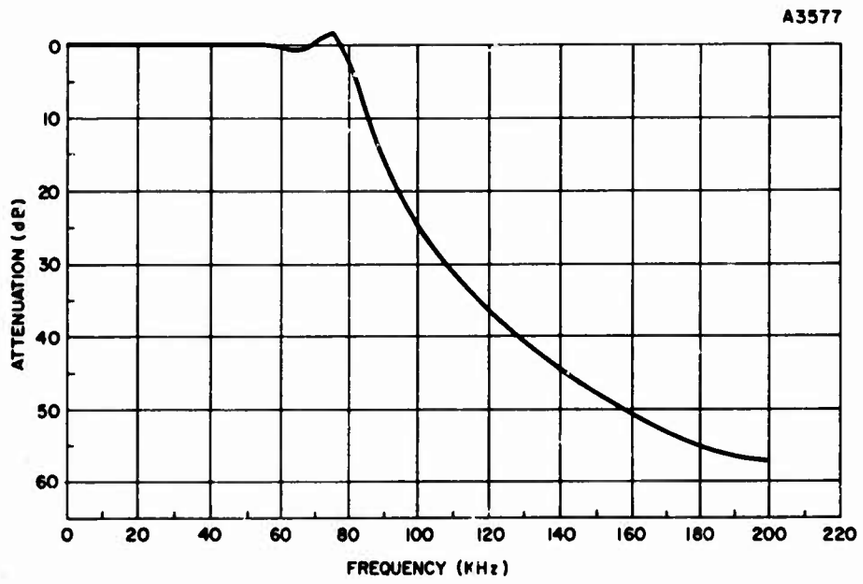


Figure 64. Frequency Response of Sideband Filters

SECTION IX

TEST AND COMMUNICATIONS EQUIPMENT

The two new remote sites are being supplied with the basic test and communications equipment necessary for efficient operation. In addition to the list of equipment provided in Interim Report No. 1, one Loran-C test signal simulator has been supplied. It will be rotated among the sites for the purpose of testing and calibrating the Loran-C timing receiver.

SECTION X

AZIMUTH OF ARRIVAL EQUIPMENT

1. INTRODUCTION

The purpose of the azimuth of arrival experiment is to identify certain HF propagation characteristics and, where possible, correlate this information with other known phenomena (sunspot activity, aurora storms, and the like). The experiment is discussed in detail in Interim Report No. 2.[1]

The basic equipment to make these azimuth of arrival measurements was provided by General Electric under Contract AF30(602)-3198. A treatment of the functional measurement technique is presented in Interim Report No. 5.[10] With this in mind, the basic goals of the equipment modifications for the azimuth of arrival experiment are:

1. To prepare the equipment for interface with automatic data collection system presently being installed, and
2. During the interim data collection period, to take those steps necessary to collect data and validate the collection technique.

At the start of the present contract, it was determined that a modified gate generator would satisfy the requirements for interface with the automatic system. Also, trial and error data collection and reduction would establish data rates and collection techniques. This would satisfy the interim requirements.

However, equipment investigations prompted by unexpected experimental results uncovered certain problems that would not be solved by the modified gat generator. The required features of the modified gate generator were incorporated he forward automatic gain control and the mode processor instead of providing a separate piece of equipment. This investigation uncovered a definite need for recalibration of the antenna system. However, the impending move to Starr Hill would minimize the worth of any flight tests for recalibration at Stockbridge; therefore, these tests were not performed.

2. DATA COLLECTION AND ANALYSIS PROBLEMS

Data from World Days before and after the azimuth antenna calibration period (August 1965) were consistent with expected trends. The flight tests basically corroborated the predicted interferometer pattern (with a shift in boresight, due to extra cable length in one side). The foldover angles did not change in proportion to the frequency; however, the total coverage was uniform and this irregularity was acceptable.

Azimuth data collection and reduction for the latter part of 1965 and the first few months of 1966 had shown the predominant receive angle to be significantly west of the great circle path to Coco Solo. The paths were received from 198° to 200° bearing instead of the previously measured and expected 187.5° bearing. In order to verify these data, CW tests were conducted on 2-3 March to locate the boresight of the Wullenweber antenna bays being used. These tests were made by transmitting a CW signal from a point on a road a few miles south on a great circle bearing of 187.5°. The intention was to compare the phase of the receive signal at the outputs of the two antenna bays, and thereby determine the phase center of the interferometer. Low signal level prohibited fulfillment of the desired tests; however, these tests did show a distinct gain difference between the antenna bays, with the eastern bay being deficient. To solve both problems (faulty eastern bay and apparent western angle of arrival), the antenna system was switched from the 150° bay to the 170° bay and the 210° bay was retained. This produced a shift in system boresight from 183.5° to 192.4° and a 46 percent increase in angular coverage. Subsequent data collection showed reception was still predominant at 200°. The CW gain tests were not repeated for the 150° bay so gain variations between the bays could not be evaluated further. The modified antenna system did not seem to offer any particular advantage thus we went back to the original Wullenweber arrangement.

The above results generated concern that the performance of the Wullenweber antenna system had changed since calibration in August 1965. Local antenna inspections and tests showed no discrepancies.

Resolution of this problem could only be achieved by scheduling aircraft recalibration flights. It was not worth while to do this because of the long lead time needed for scheduling flights and the impending move to new antennas at Starr Hill.

In order to more closely identify the data collection problem areas, the two Phantom receivers associated with azimuth of arrival were returned to General Electric for alignment and evaluation. After careful alighment, the following test was conducted to determine the effect of signal strength on the phase response of the receivers (due to AGC action) -- a block diagram of the test setup is shown in Figure 65. The following steps were performed:

1. Set pads to deliver 100 μv rms to each receiver.
2. Null phase with receiver tuning
    a. Remove B input to oscilloscope, set Boonton (via calibration knob on oscilloscope) for 1 v rms.
    b. Replace B, remove A, set Boonton to 1 v rms.
    c. Replace A, measure difference.

d. Null receivers (via tuning) until difference is a minimum.

e. Record amplitude.

3. Vary amplitude of receiver B ± 20 dB in steps of 5 dB, repeat steps 2a, 2b, 2c, and 2e.

4. Repeat 3 for receiver A ± 20 dB in 10-dB steps.

5. Repeat 1 through 4 for each frequency of interest (11.3, 16.6, and 22.5 MHz).

6. Convert difference amplitude output (as measured on Boonton) to phase by referring it to the 1-v rms normalizing level.

7. Plot the resulting family of curves for each frequency.

These curves are plotted in Figures 66 (11.3 MHz), and 67 (16.6 MHz), and 68 (22.5 MHz). The ordinate is in actual degrees phase shift and the abscissa is in relative signal strength in dB. When applying these curves to the azimuth, it is necessary to account for the interferometer conversion characteristic (0.22 for 11.3 MHz, 1.11 for 16.6 MHz, and 0.07 for 22 MHz). Thus, the ordinate should be multiplied by the appropriate coefficient to obtain the receiver's influence on the actual angle of arrival. It may be noted that for most of the usable range, the effect of the receivers on actual angle of arrival is less than 0.5°; however, when the signal level gets low (although still in receiver AGC range), significant angle bias errors crop up. These errors can be in excess of 1° and 2° actual.

Two steps have been taken to prevent this potentially erroneous data from spoiling good data. Amplitude information of the signals is being monitored to permit proper identification of weak signals. In the future, the threshold on the forward AGC can be adjusted to prevent too weak signals from being phase detected -- unless it is done knowingly and willfully, because only weak signals are present.

The rapid fluctuations of azimuth data proved to be too tedious to reduce manually. To alleviate this situation, during the interim period of manual operation, a long time constant integrator (six seconds) was placed on the output of a boxcar, and this filtered output was recorded on the Sanborn, together with the unfiltered output -- this technique proved quite successful.

Initial testing of manpower requirements to operate the angle of arrival equipment in its automatic mode indicated that the external gate could be set by the operator as he set the gates for the mode loss and polarization experiments. However, subsequent testing proved that the path time of arrival changed so fast (over a small range) that the operator would have to spend too much time placing the gates. In effect, this would require an additional operator. To combat this problem it was proposed to modify the azimuth of arrival equipment with a forward AGC loop. This, coupled with a wider sample gate on the mode processor, will minimize operator care.

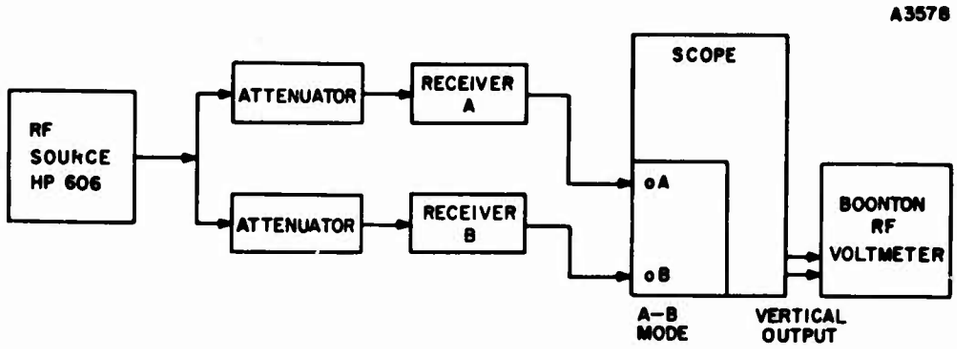


Figure 65. Receiver Phase Test Setup

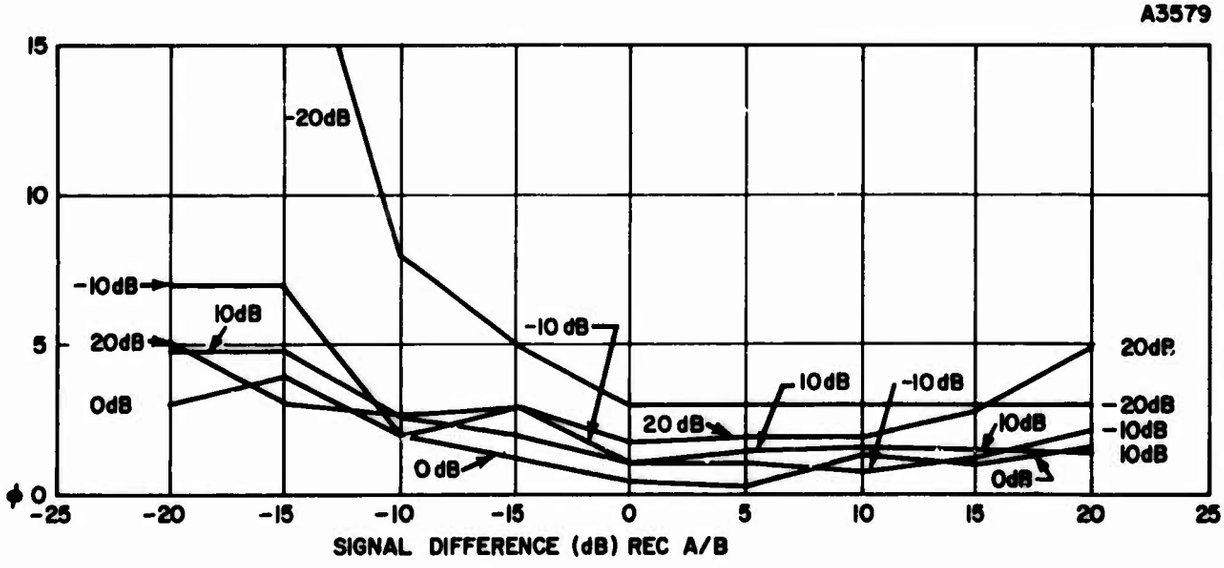


Figure 66. Phase Response, 11.3 MHz

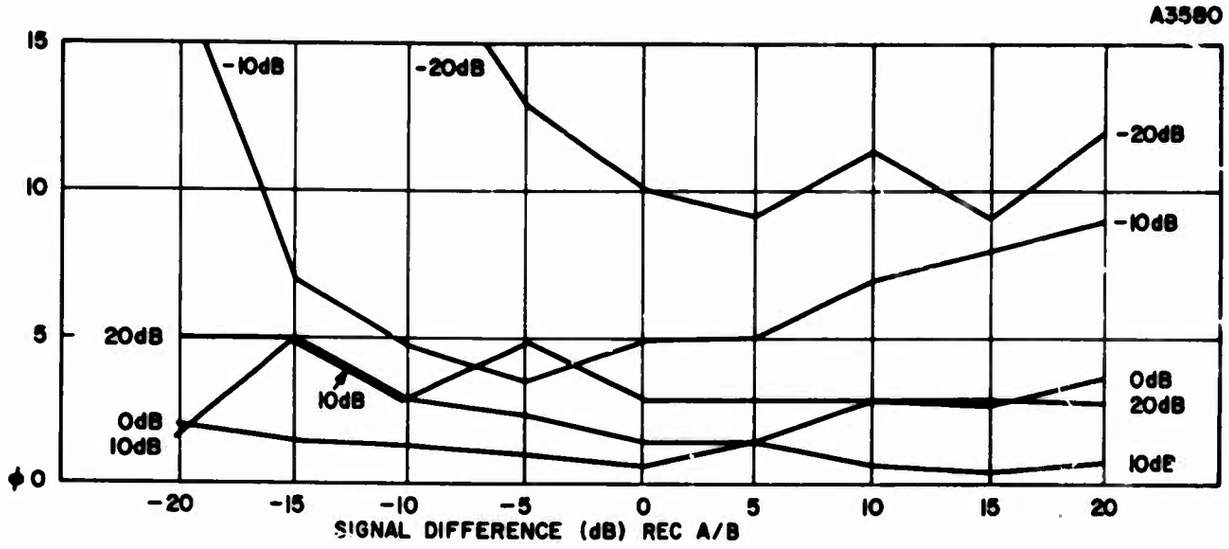


Figure 67. Phase Response, 16.6 MHz

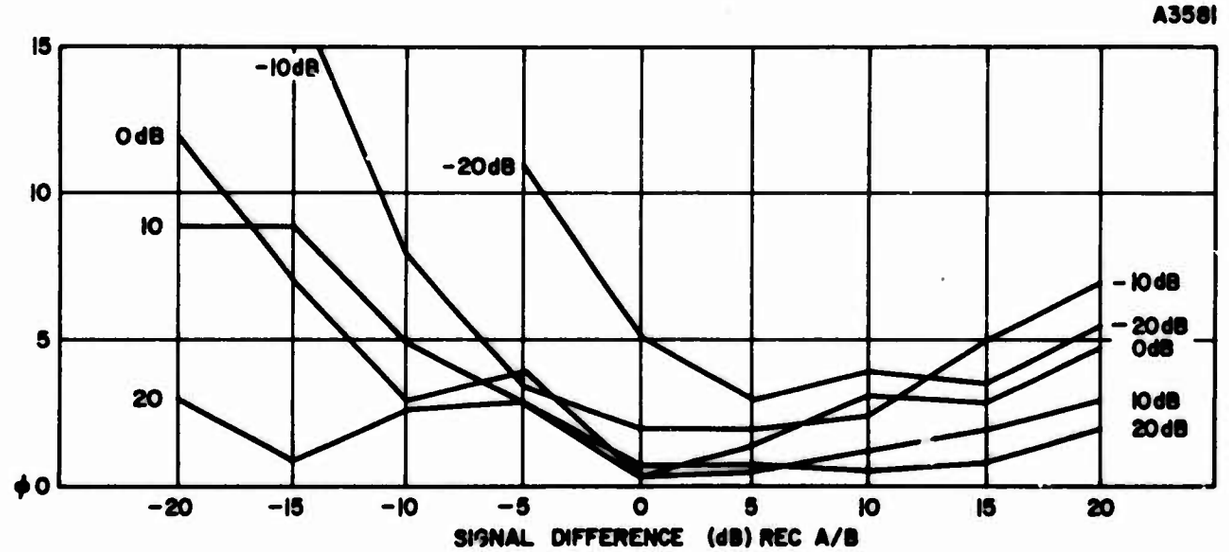


Figure 68. Phase Response, 22.5 MHz

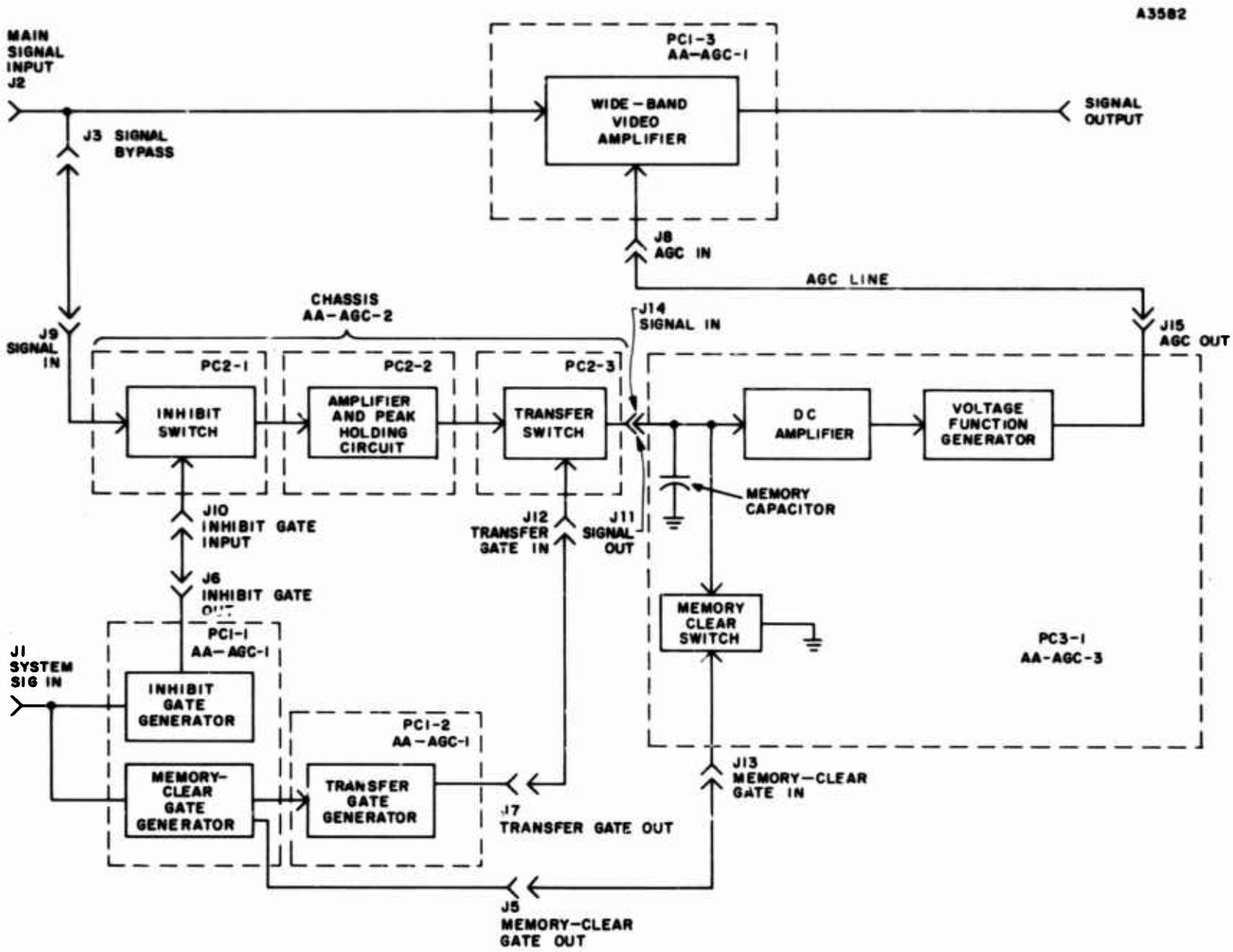


Figure 69. Forward AGC, Block Diagram

Basically the data collection difficulties to date may be summarized as follows:

1. Wullenweber antenna system performance appears to have changed since the aircraft calibration.
2. Local terrain may distort the azimuth of arrival.

(Both of these problems will be alleviated after the move to Starr Hill.)

3. Low amplitude signals will get into poor phase region of the phantom receivers.

(The automatic data collection system will inhibit low amplitude signals by means of a threshold device incorporated in the forward AGC unit.)

3. DESIGN OF FORWARD AGC

The Phantom receiver compresses the 80 dB of dynamic range into 25 dB of variation at the output (pulse mode). Because the time sidelobes of the pulse compressed waveform are less than 20 dB below the main lobe, there would have been false grating of the grated phase detector by these sidelobes. This liability would seriously hinder automatic data collection and require significant operator monitoring in order to guarantee useful data collection.

To reduce this problem, General Electric implemented a forward AGC loop in the threshold circuit of the gated phase detector. This forward loop compresses the 25 dB of variation into less than 9 dB of variation. This was accomplished by scanning a PRF sweep for the largest target present and then using a detected version of this target to set the gain for the next pulse period (forward loop AGC). This type of AGC must be employed to prevent sidelobe thresholding which would occur if conventional AGC were used (because the all-too-high sidelobes precede the even higher main lobe).

In the forward AGC, the output of the matched filters is fed into a peak detector. At the end of a pulse period the detector output is passed on to a holding circuit. Then the detector is cleared and ready for the next pulse. The holding circuit then converts the detected voltage to a suitable range for the AGC amplifier which is a complementary pair video amplifier. This voltage is held for the next entire pulse period at the end of which it is dumped in preparation for the new AGC level. Although this system does not provide exact amplitude information, the required compression will be accomplished. The system shown in Figure 69 will use integrated circuits to keep the size small and the reliability high. Each of these circuits will now be discussed individually.

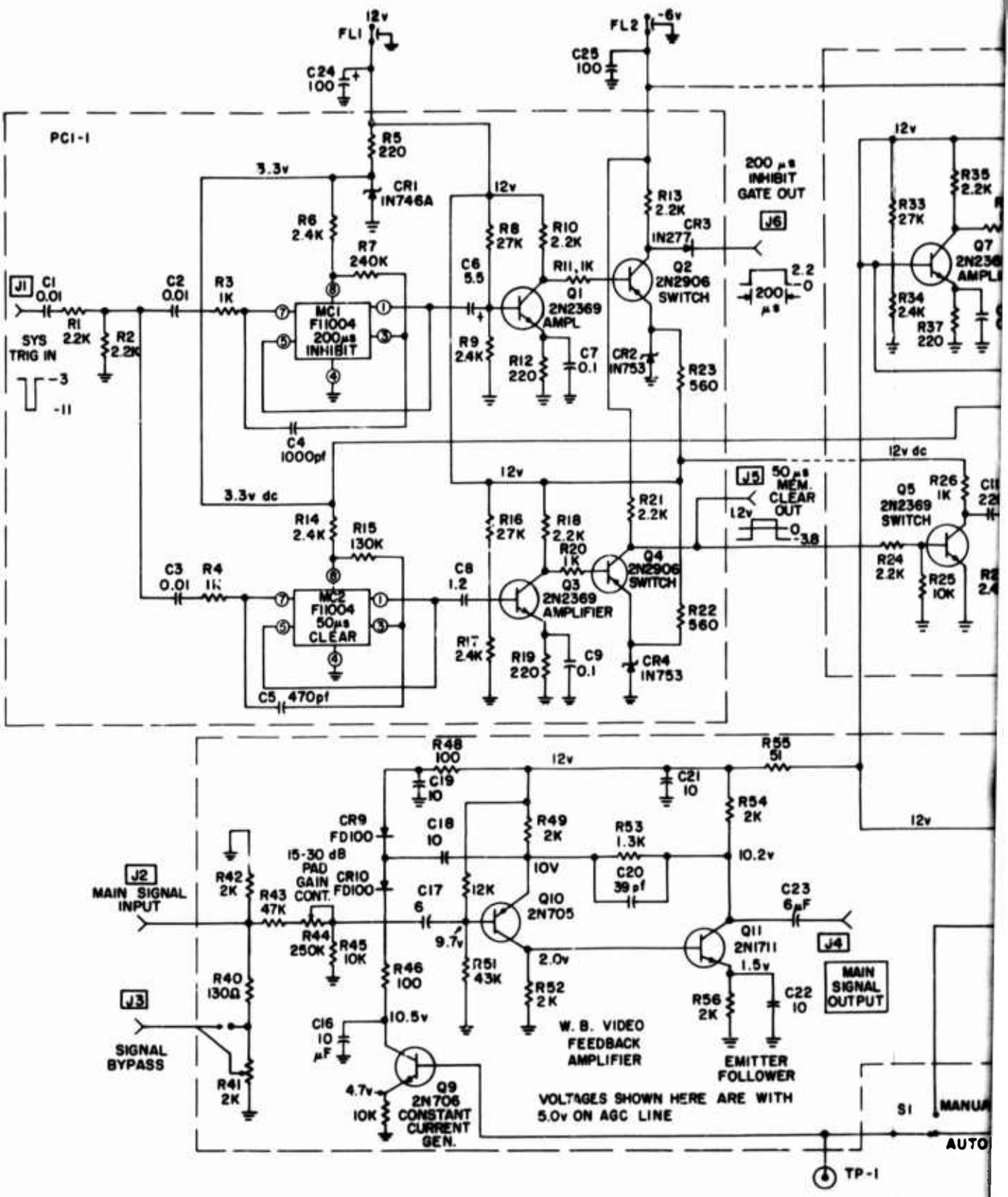
a. PC1-3 Main Signal Amplifier

The PC1-3 is a wide-band video feedback amplifier consisting of two transistor stages. Its 3-dB pass-band extends from approximately 200 Hz to 3 MHz (see Figure 70). The upper 3-dB break frequency is determined by R53 and C20. The lower 3-dB break frequency is determined by the large coupling and bypass capacitors, such as C17, C22, and C18.

The gain control characteristic of the amplifier is shown in Figure 71, and is a function of the effective diode resistance of CR9 and CR10. The diode resistance is in parallel with unbypassed emitter resistor R49 of Q10; therefore, the effective emitter resistance will vary as a function of the diode resistance. When CR9 and CR10 are back-biased the effective emitter resistance of Q10 is just the value of R49 (2000 ohms). As the diodes become forward-biased, the emitter resistance soon is entirely due to the diode resistance.

Diodes CR9 and CR10 are directly coupled to Q9, which acts as a constant-current generator. When the base voltage of Q9 is zero or negative, the transistor is cut off and diodes CR9 and CR10 are effectively back-biased. The effective emitter resistance of Q10 is then 2K, and the amplifier gain is very low. As base drive is applied to Q9, CR9 and CR10 become forward-biased, diode resistance decreases, and the effective emitter resistance of Q10 decreases. The amplifier gain therefore increases. Diode resistance decreases with increasing positive drive on Q9 until saturation of Q9 occurs. Once saturation is reached no further AGC control is available.

Since we want to AGC this amplifier, we must initially start at some particular value of gain level and then (in the presence of large signals) reduce the gain with AGC. From Figure 71, it is noted that a total of 6 to 30 dB (24 dB) of AGC control is available from a 0.5-v to 7-v bias. Since only a 16-dB range is desired, an operating range between 0.9 and 5 v of bias was chosen, thus allowing a little extra control if needed. Under small signal conditions the required AGC standing bias is 5 v to maintain the amplifier at a 27-dB level. When AGC starts, the control bias must follow the curve of Figure 71 and the end bias voltage must be 0.9 v for the full 16-dB AGC range. The detector circuits are therefore responsible for implementing the control voltage in such a fashion that output signal level of the main amplifier will be nearly constant during the AGC period.


PC1-1
FL1
12v
FL2
-6v
C24 100
C25 100
R5 220
3.3v
CR1 IN746A
R6 2.4K
R7 240K
J1 C1 0.01
SYS TRIG IN
-3
-11
R1 2.2K
R2 2.2K
C2 0.01
R3 1K
MC1 F11004 200µs INHIBIT
C4 1000pf
C6 5.5
R8 27K
R10 2.2K
R11 1K
Q1 2N2369 AMPL
R9 2.4K
R12 220
C7 0.1
R13 2.2K
CR3 IN277
Q2 2N2906 SWITCH
CR2 IN753
R23 560
200 µs INHIBIT GATE OUT
J6
2.2
0
200 µs
12v dc
3.3v dc
R14 2.4K
R15 130K
C3 0.01
R4 1K
MC2 F11004 50µs CLEAR
C5 470pf
C8 1.2
R16 27K
R18 2.2K
R20 1K
Q3 2N2369 AMPLIFIER
R17 2.4K
R19 220
C9 0.1
R21 2.2K
Q4 2N2906 SWITCH
R22 560
CR4 IN753
J5 50 µs MEM. CLEAR OUT
12v
0
-3.8
Q5 2N2369 SWITCH
R26 1K
R24 2.2K
R25 10K
R33 27K
R35 2.2K
Q7 2N236 AMPLI
R34 2.4K
R37 220
R48 100
C19 10
C21 10
R55 51
R54 2K
CR9 FD100
C18 10
R49 2K
R53 1.3K
15-30 dB PAD GAIN CONT.
CR10 FD100
10V
10.2v
C20 39 pf
J2 MAIN SIGNAL INPUT
R42 2K
R43 47K
R44 250K
R45 10K
C17 6
12K
Q10 2N705
9.7v
C23 6µF
Q11 2N1711
1.5v
J4 MAIN SIGNAL OUTPUT
R40 130Ω
J3 SIGNAL BYPASS
R41 2K
R46 100
R51 43K
2.0v
R52 2K
R56 2K
C22 10
C16 10 µF
10.5v
4.7v
10K
Q9 2N706 CONSTANT CURRENT GEN.
W. B. VIDEO FEEDBACK AMPLIFIER
EMITTER FOLLOWER
VOLTAGES SHOWN HERE ARE WITH 5.0v ON AGC LINE
S1
MANUA
AUTO
TP-1

1

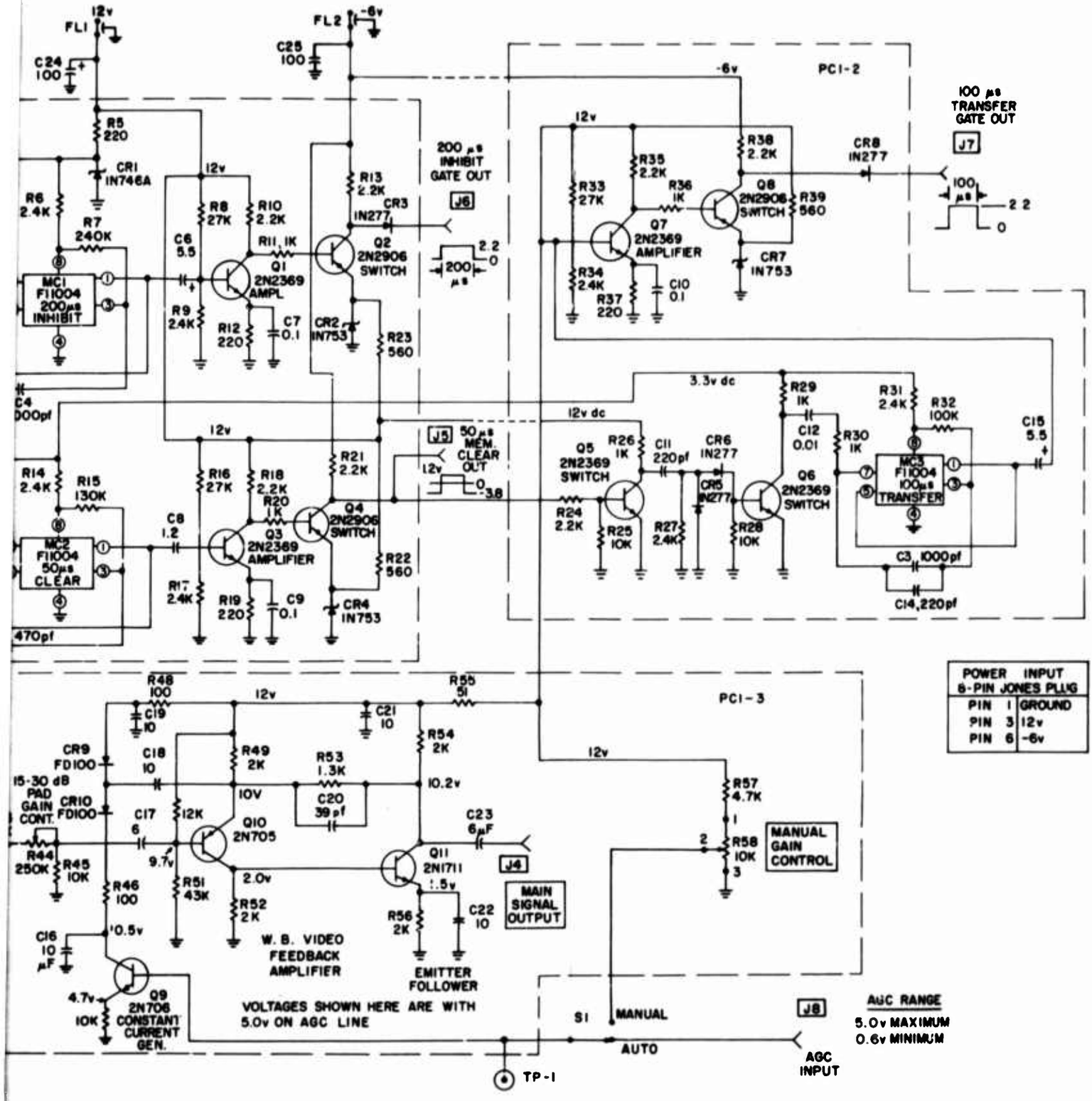


Figure 70. Printed Circuit 1

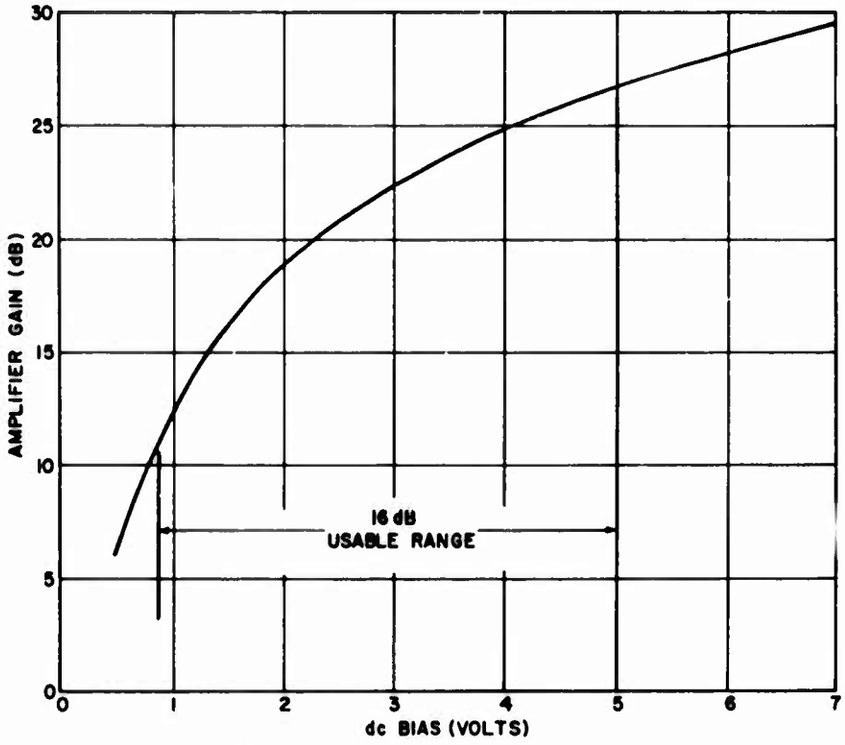


Figure 71. Gain Control Characteristic

b. PC2-1 Inhibit Switch

The main bypass signal input at J9 is fed to amplifier Q16 on PC2-1 (shown in Figure 72) and passed by the diode gate composed of CR11 to CR14. This gate is normally open (that is, it passes signals) except for the 200-μs duration of the inhibit gate pulse which closes it.

c. PC2-2 Pulse Amplifier and Peak Holding Circuit

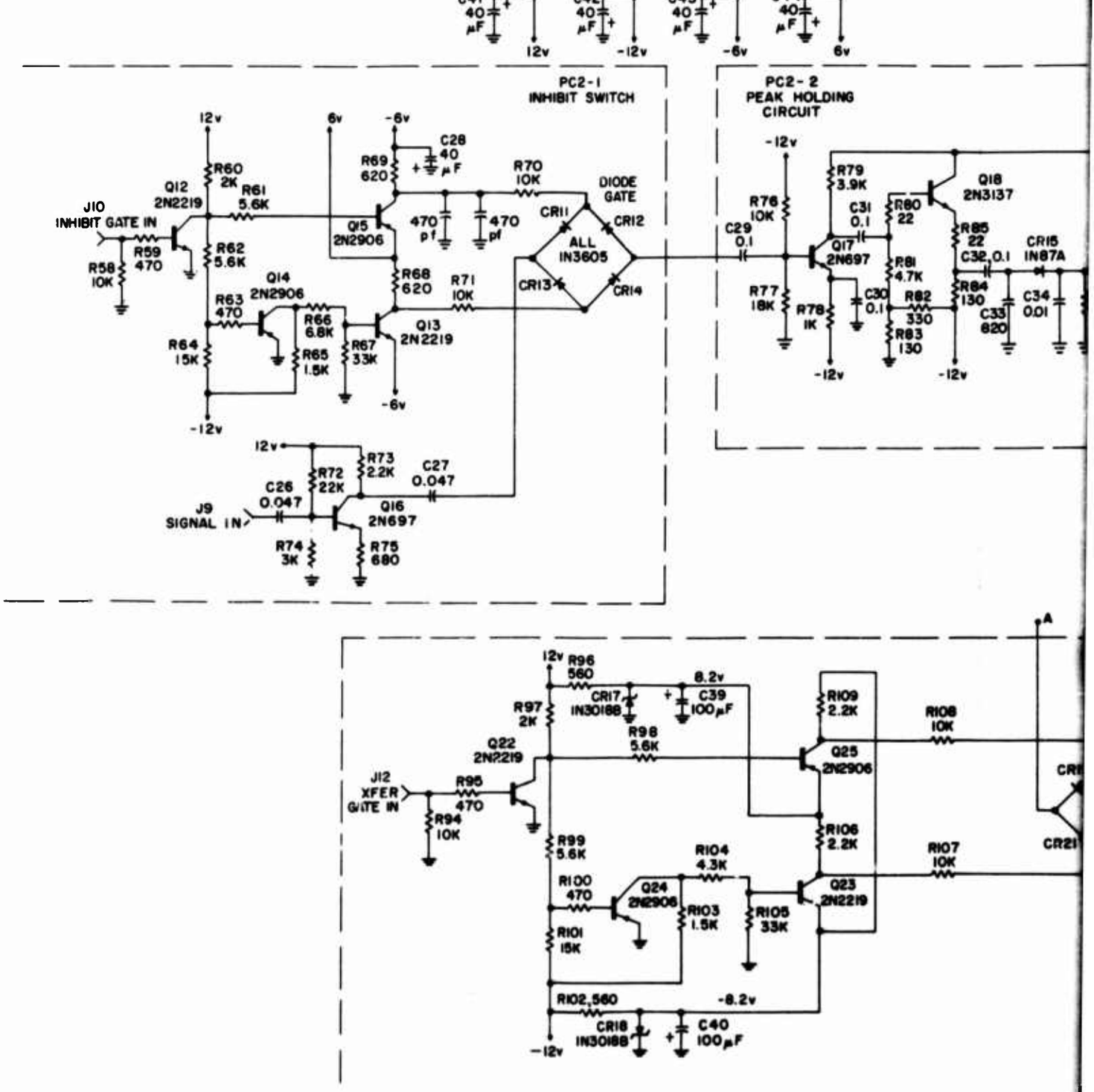
After passing through the inhibit gate the main bypass signal is further amplified by Q17 (Figure 72). Q18 is an emitter follower used to drive detector diode CR15. The rectified signal is filtered by C34 and R16 and further amplified by Q19. Q20 is an emitter follower used to supply the drive for Q21. Q21 in turn charges the peak holding capacitor C38. C38 (0.1 μf) is a compromise value for good response to signals of pulse widths of 10 μs, or less, and high time constant (TC) for negligible droop. C38 charges to the peak voltage level of the incoming video pulse. When C38 is charged, the base-emitter diode of Q21 is effectively back-biased so that C38 cannot discharge through it. Q21 will then only conduct when the input signal is larger than the charge on C38. The dynamic range of this circuit is determined by the static voltage characteristics of Q21. The minimum turn-on signal is about 0.7 v and the maximum signal is determined by the base-emitter breakdown voltage BV_{BEO}. In most transistors BV_{BEO} is on the order of 5 to 7 v, which limits the dynamic range to somewhat less than 20 dB. Q21 in this case is a 2N1234 transistor with high breakdown voltage that does not limit the dynamic range.

The charge on C38 can also discharge through the transfer gate composed of CR19-CR22. However, the resistance looking into the gate when this gate is closed (no signal passes) is on the order of several megohms; therefore, the discharge time constant of C38 and parallel resistance of Q21 and diode gate is greater than 500 ms. It is only necessary for C38 to hold its charge for one pulse period of 5 ms; therefore, there is no appreciable droop of the dc voltage held by C38.

d. PC2-3 Transfer Switch

The dc voltage from the peak holding circuit is transferred through the transfer gate during the 100-μs transfer period. The transfer gate is applied to the bipolar complementary pulse circuit composed of Q22, Q23, Q24, and Q25 (Figure 72).

To realize the full dynamic range of the peak holding circuit it was necessary for the output voltage swing of Q23 and Q25 to be at least 8 v. The positive 8 v was derived from R96, C39, and zener diode CR17; the negative 8 v from R102, C40, and zener diode CR18.


12v
FL1
-12v
FL2
6v
FL3
-6v
FL4
C41 40 μF
C42 40 μF
C43 40 μF
C44 40 μF
PC2-1
INHIBIT SWITCH
PC2-2
PEAK HOLDING
CIRCUIT
J10
INHIBIT GATE IN
R58 10K
R59 470
Q12 2N2219
R60 2K
R61 5.6K
R62 5.6K
Q15 2N2906
R69 620
C28 40 μF
R70 10K
DIODE GATE
CR11
CR12
CR13
CR14
ALL IN3605
470 pf
470 pf
R68 620
R71 10K
Q14 2N2906
R63 470
R66 6.8K
R64 15K
R65 1.5K
R67 33K
Q13 2N2219
J9
SIGNAL IN
C26 0.047
R72 22K
R73 2.2K
C27 0.047
Q16 2N697
R74 3K
R75 680
C29 0.1
R76 10K
R77 18K
R78 1K
R79 3.9K
Q17 2N697
C31 0.1
C30 0.1
R80 22
R81 4.7K
R82 330
R83 130
Q18 2N3137
R85 22
R84 130
C32 0.1
C33 820
CR15 IN87A
C34 0.001
R96 560
CR17 IN3018B
C39 100μF
8.2v
R97 2K
R98 5.6K
Q22 2N2219
J12
XFER GATE IN
R95 470
R94 10K
R99 5.6K
R100 470
Q24 2N2906
R101 15K
R103 1.5K
R104 4.3K
R105 33K
R109 2.2K
R108 10K
Q25 2N2906
R106 2.2K
R107 10K
Q23 2N2219
R102 560
CR18 IN3018B
C40 100μF
-8.2v
A
CR21

1

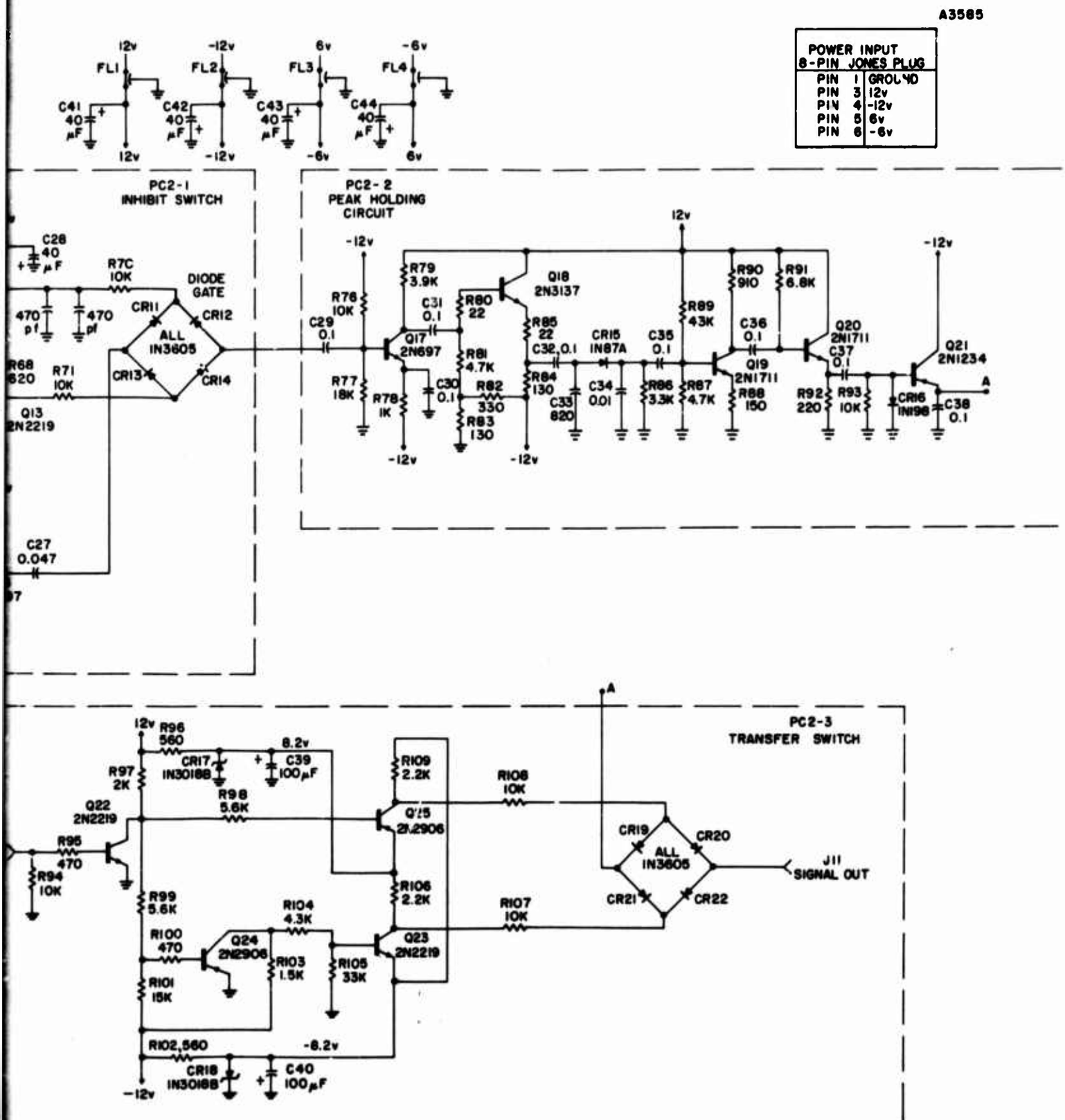


Figure 72. Printed Circuit 2

e. PC3-1 DC Amplifier and Function Generator

The dc voltage from the peak holding circuit is transferred through transfer gate to the memory capacitor C45. At the end of the 100-μs transfer period, C45 holds this charge until the next pulse period. The peak holding capacitor, however, is now ready to accept new information.

Q26 and Q27 (shown in Figure 73) comprise the memory clear switch which discharges C45 at the end of each pulse period. The 50-μs memory clear pulse is applied at J13. Q26 is a voltage level changer to set the proper on-off conditions for Q27. The C45 memory capacitor must hold its voltage level for a full pulse period of 5 ms. The discharge time constant must be high and, in order to achieve this, field effect transistor (FET) Q28 is used as a source follower (similar to emitter follower) to provide high input resistance at the gate terminal. The resistance can be and usually is greater than 10 megohms. The discharge time constant, however, is determined by the parallel resistance of R_{IN}(FET), R (diode gate), and R (Q27). This TC, however, is still quite high with only negligible droop (less than 5 percent).

The source follower Q28 drives a dc amplifier, μA702C, which is a linear integrated microcircuit. It is a high gain dc amplifier which is used as an operational amplifier. In this configuration, the gain is a function of the ratio of feedback resistance R122 and input resistance R116.

The dc amplifier, therefore, has a gain determined by the ratio of R122 to R116 or $\frac{22\ K}{4.7K} \approx 5$ which is about 14 dB.

This boosts the detected voltage to a higher level for further shaping in the function generator. Figure 74 shows the output voltage as a function of input signal level.

The dc amplifier drives emitter follower Q29. Biasing here is important because we want the base of Q29 to be very close to zero under no-signal conditions, otherwise, the dc amplifier (μA702C) will be supplying base drive to Q29 under all conditions. The dc voltage that appears at the emitter of Q29 is the working voltage that must be transformed into a voltage characteristic that will match the main signal amplifier AGC characteristic over the required dynamic range. We have already decided that the main signal amplifier AGC characteristic will vary from 5 v at minimum signal to 0.9 v at maximum signal as shown in Figure 71.

Figure 75 is a plot of dc voltage out as a function of signal level at the emitter of Q29. Figures 71 and 75 both show input signal variations of 16 dB over which significant output level changes are evident. If required dc bias (from Figure 71) is plotted as a

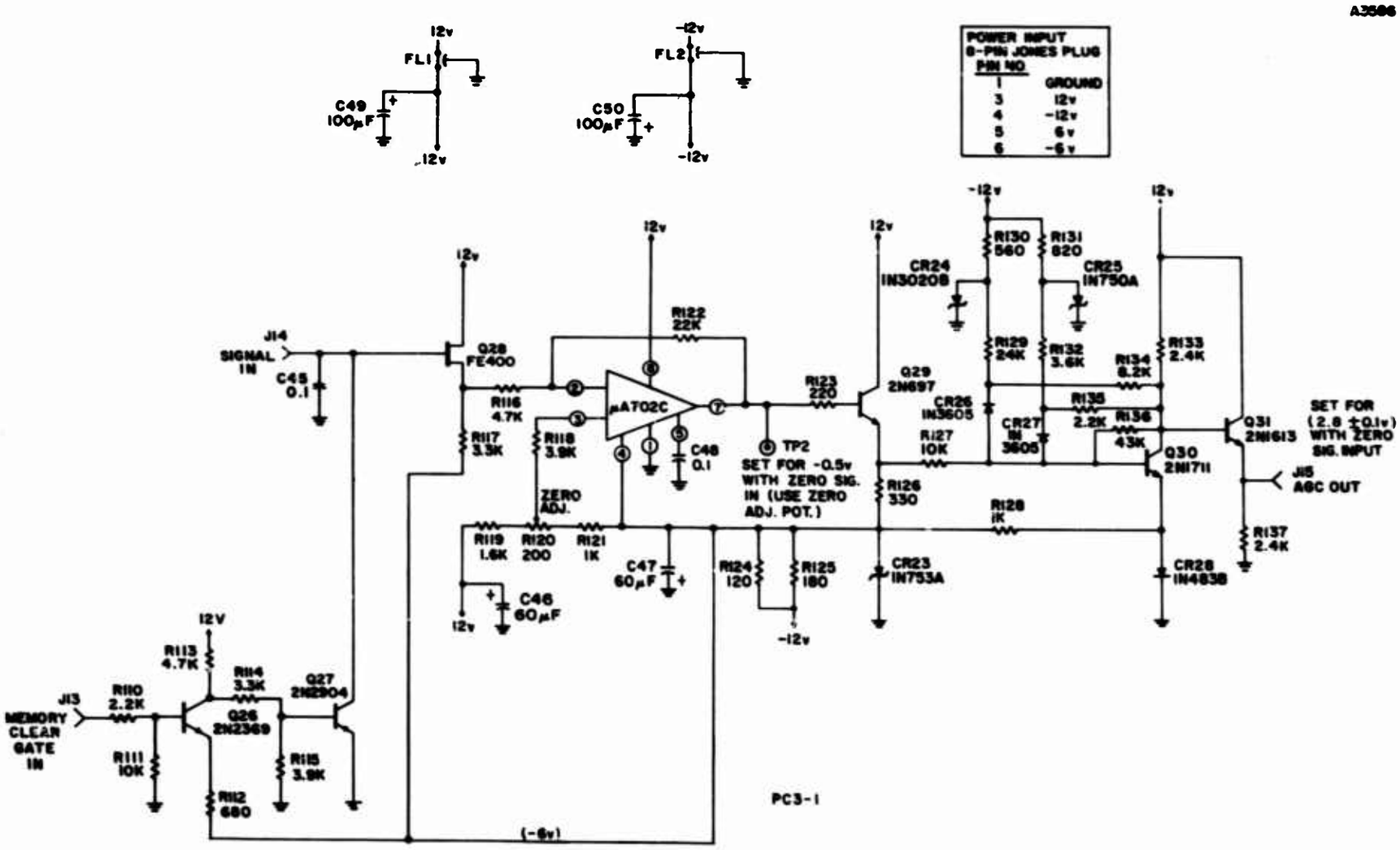


Figure 73. Printed Circuit 4

function of actual dc level change (from Figure 75) in 2-dB signal level increments over the 16-dB AGC range, the resulting plot contains the information necessary to design function generator Q30.

Figure 76 shows this information plotted. Each point represents a 20-dB increment of change in signal level and the corresponding AGC voltage necessary to maintain the output signal at a constant level. Figure 76 actually tells us the gain function of the function generator necessary to arrive at the proper AGC function to control the main signal amplifier.

Gain is defined as the slope of the input-output curve. Figure 77 shows the line segment approach to synthesizing the gain curve. Segment No. 1 covers a signal range from -16 to -13 dB. The gain is determined by the ratio of the change in output dc level to change in input dc level over the 3-dB signal change; in this case the gain slope is 4.3. Segment No. 2 covers a signal range from -13 to -7 dB; the gain slope here is 0.7. Segment No. 3 covers the signal range -7 to 0 dB for a gain slope of 0.15.

Function generator Q30 is a high beta 2N1711 transistor operating as an operational amplifier. In this type of amplifier, the voltage gain is determined by the ratio of feedback resistance to input resistance. The input resistance is 10K (R127) and the feedback resistors are R134, R135, and R136.

The initial gain slope of 4.3 of segment No. 1 is determined by the ratio of R136 (43K) to R116 (10K). Segment No. 2 breaks in at a dc level of 2.1 v. Diode CR26 is biased off until the collector of Q30 falls to 2.1 v, the gain slope is then determined by resistors R136 (43K) and R134 (8.2K) in parallel.

Segment No. 3 is determined by the back-bias on diode CR27. When the collector of Q30 falls to approximately 1.2 v, the gain slope will be determined by resistors R134, R135, and R136 in parallel.

Transistor Q30 (function generator) is direct-coupled to emitter follower Q31, which in turn drives constant current generator Q9 on PC1-3.

Figure 78 shows the output versus input voltage transfer characteristic of the angle of arrival AGC system. The output signal level is held constant within ±1 dB for an input signal level increase of 16 dB.

f. PC1-1 Inhibit and Memory-Clear Gate Generator

The timing waveforms are shown in Figure 79. The system trigger initiates simultaneously the 200-μs inhibit gate and the 50-μs clear gate.

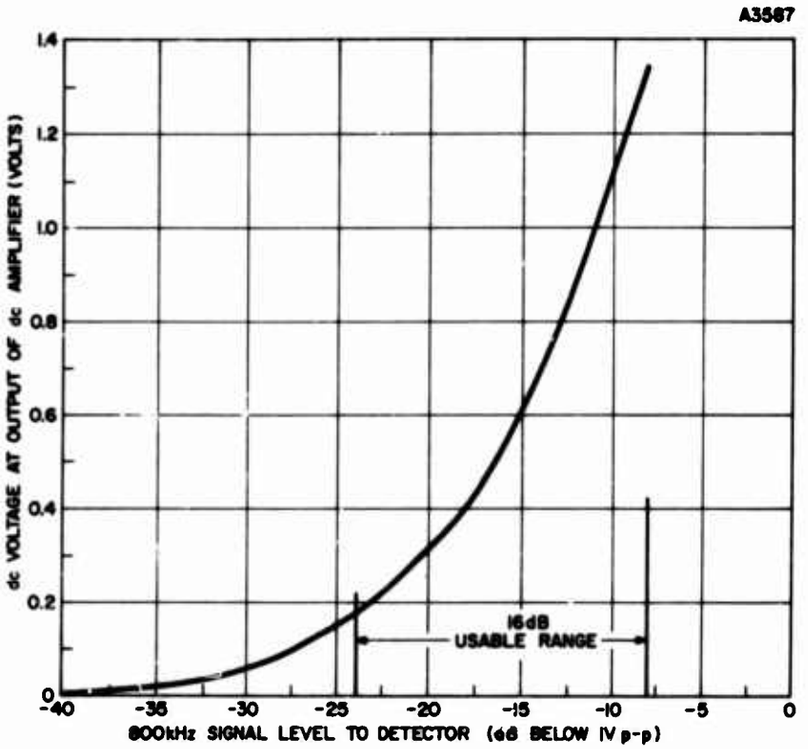


Figure 74. dc Amplifier Output

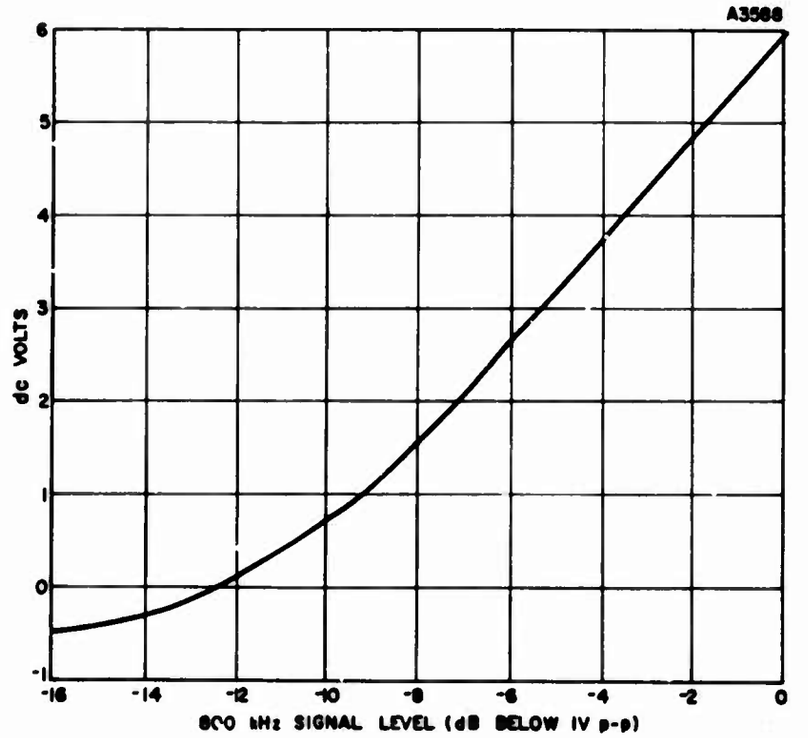


Figure 75. Emitter Follower Output

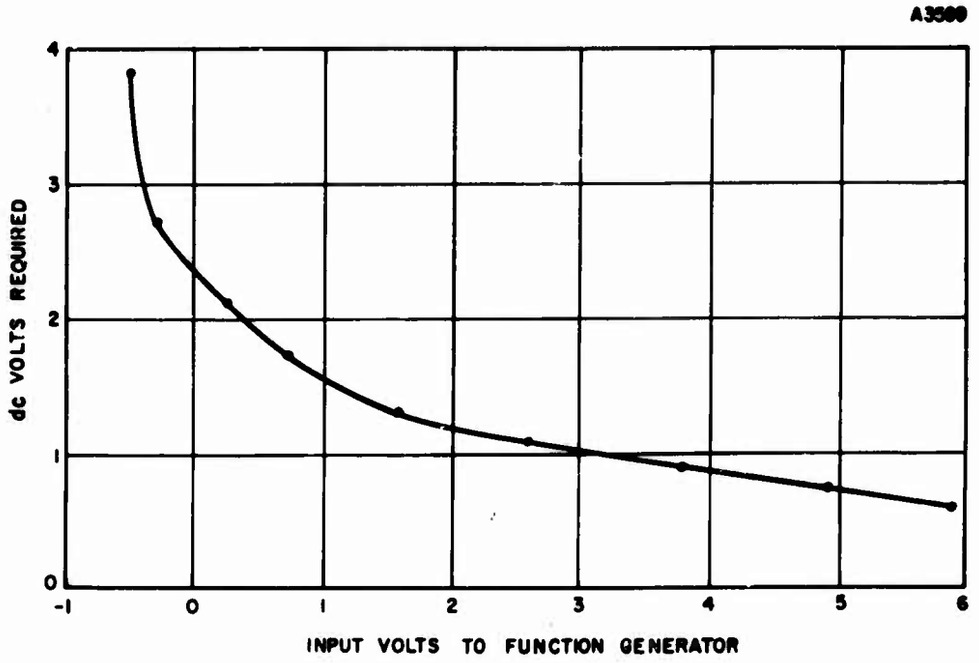


Figure 76. Required Gain Characteristic

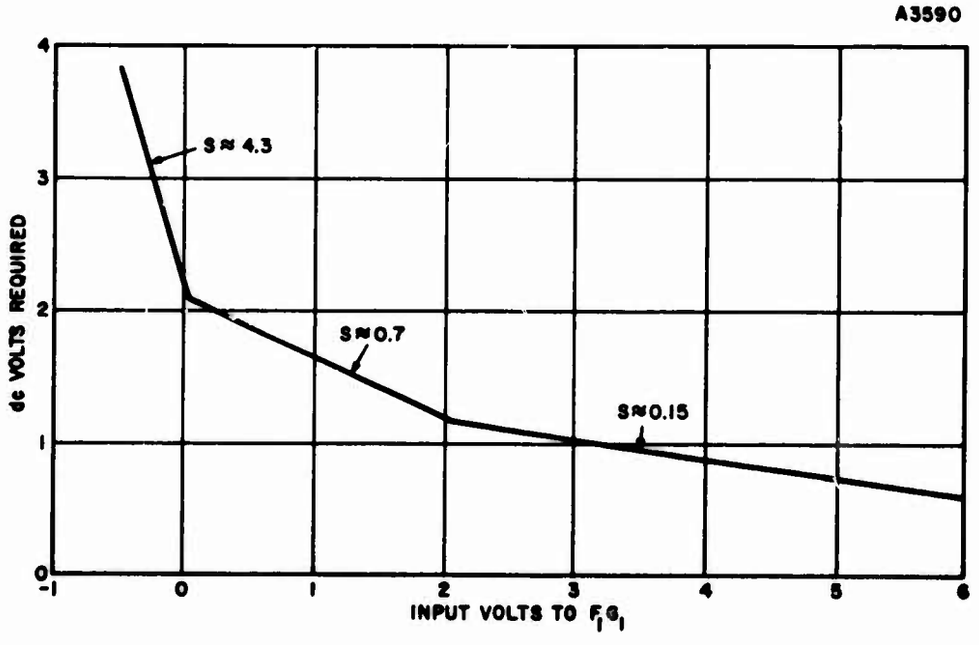


Figure 77. Line Segment Approach to Synthesis

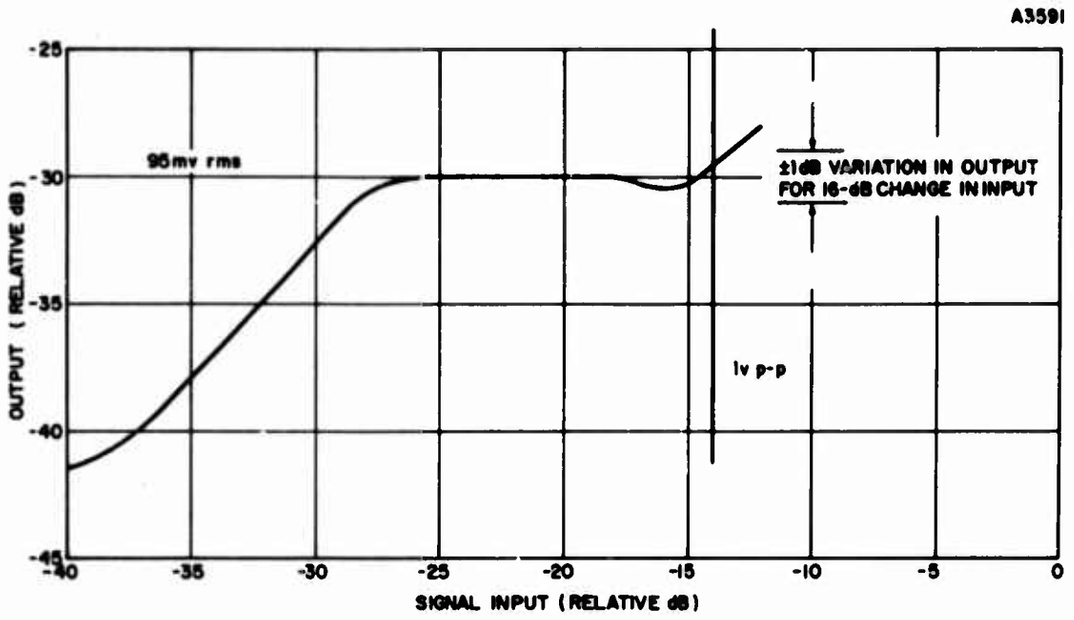


Figure 78. AGC Characteristic

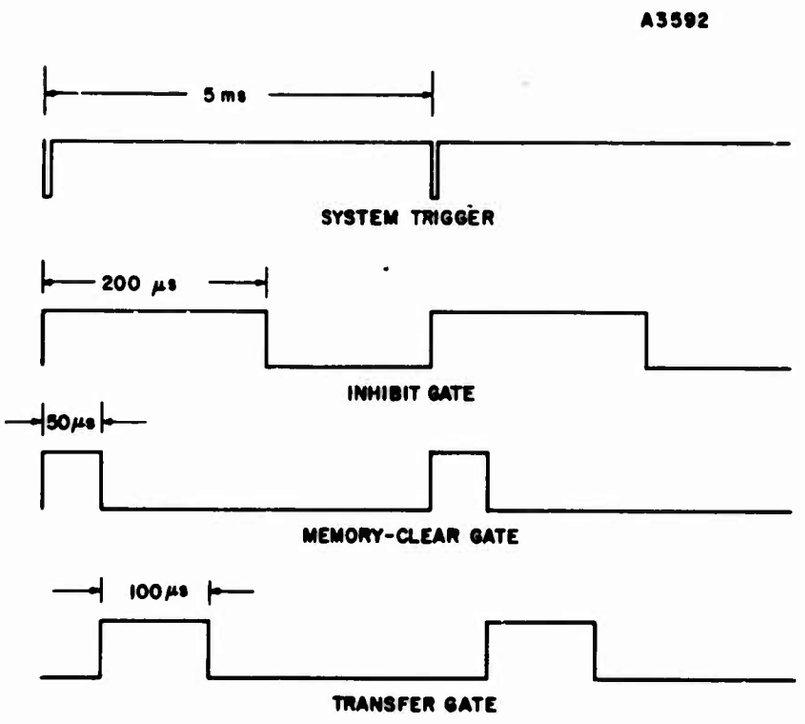


Figure 79. Timing Waveforms

Amelco F11004 micro-logic elements are used as one-shot monostable multivibrators whose pulse width is determined by an RC time constant. The output pulses from MC1 and MC2 are too low in amplitude to directly drive the dual gate generator on PC2-1 (inhibit switch) and PC2-3 (memory-clear switch). Amplifiers Q1 and Q3 (shown in Figure 70) amplify the gates to drive switches Q2 and Q4 into saturation. Switches Q2 and Q4 are primarily level changers necessary to switch the dual-gate generators mentioned.

g. PC1-2 Trigger Delay

The 50-μs memory-clear gate generated on PC1-1 is again changed in level by Q5 (shown in Figure 70) and differentiated by C11 (220 pf) and R27 (2.4K). Diode CR5 clips the negative-going spike on the leading edge and passes the positive-going trailing edge spike. This results in a trigger delay of 50 μs. The trigger is changed in level by Q5 which triggers MC3, the 100-μs transfer gate. The output of MC3 is again amplified and level changed to drive the dual-gate generator on PC2-2.

The transfer gate, therefore, transfers the charge from peak holding capacitor C38 to memory capacitor C45 immediately after the memory capacitor has been cleared of the previous charge.

h. Operating Modes

(1) Manual Gain Control

With switch S-1 in manual position, potentiometer R58 is used to vary a dc voltage on the normal AGC line.

(2) AGC-ON

With switch S-1 in ON position, functioning as a forward AGC system, TP1 can be used to monitor the AGC line or can be used to set the amplifier gain at a specified level when operating in the manual-gain control mode.

i. Test Procedure

(1) Set S-1 to AUTO. Set signal generator to 800-kHz (or use own internal signal source) and input level to J2 at 50 mv peak-to-peak. With Triplett meter, set voltage at TP-2 for -0.5 v dc by adjusting R120 zero adjust potentiometer.

(2) Move Triplett meter to TP-1 and read AGC voltage of 2.8 v. If necessary, readjust R120 zero adjust potentiometer for this voltage.

(3) Observe the main signal output (J4) on oscilloscope with a 1K termination. Input signal level must be 50 mv peak-to-peak and the AGC voltage 2.8 v. Adjust R44 gain control for 50 mv peak-to-peak across 1K load.

(4) Increase the input signal level at J2 to 1 v peak-to-peak. With Triplett meter at TP1, observe that the AGC voltage falls to approximately 0.5 v dc.

APPENDIX A

SPECIFICATION FOR ANTENNA ARRAY AT STARR HILL

SK 62667-782-11

SECTION 1. DEFINITION OF MATERIALS AND SERVICES BY PART NUMBERS

The subcontractor shall furnish parts as itemized below. Each required part shall be itemized on the purchase order.

Part 1: One antenna array formed by two vertically polarized log periodic dipole arrays and one horizontally polarized dual log periodic dipole array.

Part 2: Instruction book and installation manual delineating the equipment supplied and the proper installation procedures.

Part 3: Test data in accordance with Section 5 of this specification.

Part 4: Replacement Parts Lists for the service and maintenance of this equipment.

SECTION 2. GENERAL REQUIREMENTS

2.1 This specification governs the engineering, design and performance of the equipment to be manufactured for the Heavy Military Electronics Department, General Electric Compnay, Syracuse, New York.

2.2 This equipment shall comprise three sets of antennas for signal propagation in three directions. Figure 80 (SK 62667-984-2) identified the planned installation of the antenna arrays on Starr Hill north of Rome, New York.

Each antenna set will include two vertically polarized log periodic dipole arrays with a frequency range of 4 to 64 MHz and a horizontally polarized dual log periodic dipole array with a frequency range of 8 to 64 MHz.

The vertically and horizontally polarized antennas shall share a common center tower, and be located as close together as practical.

A ground screen extending 500 feet from the rear of the vertically polarized antennas and 8 feet above ground level will be installed but not as a part of this antenna equipment.

2.3 Deleted (see 7.1)

2.4 Deleted (see 7.1)

2.5 Approval of design concepts and layouts from General Electric Company in no way relieves the subcontractor of his responsibility to meet all the requirements of this specification.

SECTION 3. DETAILED REQUIREMENTS, SPECIFIC REPORTS

3.1 This equipment whall be designed to withstand the following environmental conditions:

Winds up to 120 mph with no ice.

Winds up to 100 mph with $\frac{1}{2}$" radial ice.

Ambient temperature range from -30°F to +95°F.

This area is subject to rain, sleet, snow and freezing rain.

3.2 Electrical Performance Requirements

3.2.1 The two vertically polarized log periodic dipole arrays shall be installed with a common apex point and two-thirds wavelength spacing at the array phase centers such that the output signal from the two arrays will not differ by more than ±2° from a constant phase or time delay error as frequency is changed when a signal is received from a direction along the bisector of the angle formed by the two arrays. These arrays will be of the type in which the phase center remains at a constant height above ground in wavelengths. This height should be as low as practical, which is a nominal one quarter wavelength. These antennas will be used in an interferometer; therefore, the motion of the phase centers of the two arrays must match.

The antennas may also be used for transmitting at a peak power of 5 kW and an average power of 2.5 kW maximum. The frequency range of the antenna shall be 4 to 64 MHz. The antenna arrays shall also have the following characteristics:

Impedance	- 50 ohms nominal
VSWR	- 2:1 maximum
Vertical pattern upper 3-dB point (over ideal ground)	- between 20° and 30°
Azimuth beamwidth	- 120° maximum
Gain	- 13 dB minimum

3.2.2 The horizontally polarized dual log periodic dipole array in each set shall have a vertical pattern determined by two curtains one-half and one wave-

length above ground. The frequency range for the antenna is 8 to 64 MHz. Other characteristics for the horizontally polarized dual log periodic dipole array are:

Power capability	- 5 kW peak 2.5 kW average
Impedance	- 50 ohms nominal
VSWR	- 2:1 maximum
Azimuth beamwidth	- between 50° and 80°
Gain	- 13 dB

3.2.3 The ground screen, although not a part of this contract, will be installed 500 feet in front of the rear towers of the vertically polarized arrays as shown in Figure 80. The slope of the ground in the vicinity of the antennas is between 0 and 10 percent. This screen will be placed eight feet (nominally) above the ground. (See 7.2)

An additional area 500 feet beyond the ground screen will be cleared of trees and obstructions as indicated in Figure 80.

3.3 Mechanical Performance Requirements

The detailed mechanical design and construction of these towers and antennas shall be accomplished subject to the requirements of this specification. Details of design and construction not specified shall conform to the best engineering practice. The requirements are detailed only to the extent considered necessary to obtain the desired performance. Any unit, item or part necessary for proper performance, in accordance with the requirements contained herein, shall be supplied even though that unit, item or part may not be specifically described or called for in this specification

3.3.1 The towers for the antenna supports shall be designed to allow for the ground screen to be placed approximately eight feet above ground level. Topography of the area for the ground screen will be available by 15 May 1966. This information will be forwarded by this date with the final slope of the ground screen determined so the antenna design can be finalized.

Front poles for the support of the high frequency end of the catenary shall not be provided as a portion of the contract.

The tower structure shall be fabricated from structural steel in accordance with A.S.T.M. Standards. Welding of tower members shall conform to accepted practices of the American Welding Society.

Unless suitably protected against electrolytic corrosion, dissimilar metals shall not be used in intimate contact with each other.

3.3.2 All iron and structural steel above ground, not to be encased in concrete foundation, shall be thoroughly galvanized in accordance with A.S.T.M. Standard A-123-47. Galvanizing shall be performed after all shop work has been completed. Any article found to have acid spots or other galvanizing defects shall be rejected.

The final paint film color shall be in accordance with existing F.A.A. Regulations and Standards.

3.3.3 Aircraft warning lights in accordance with F.A.A. Regulations are to be provided.

3.3.4 It shall be possible to replace or repair parts of the equipment easily and quickly in case of damage. A structural fuse shall be inserted in the catenary to protect the system from damage should loads in excess of design loads develop.

3.3.5 All members, assemblies and parts shall be identified by reference to erection and installation instructions provided with the antenna system.

3.3.6 All equipment shall be manufactured and finished in a thorough workmanlike manner. Parts shall be fabricated in accordance with good commercial practice.

3.3.7 In addition to the hardware required to install the antenna system, an additional 10 percent of all bolts, nuts, washers, lock nuts, etc. shall be provided with a minimum of one of each size to be provided.

3.3.8 The subcontractor shall furnish the design of all concrete footing and anchors based upon 4000 lbs/ft^2 allowable soil pressure. All anchor bolts and other materials necessary for mounting the tower, guys and longerons or lower catenary to the footings shall be provided as a part of the antenna system.

3.4 A complete set of installation instructions detailing all parts, assemblies and components supplied and their proper installation sequences shall be supplied. In addition all requirements and details for installation of footings, anchors and the wooden poles shall be provided. Periodical maintenance instruction for proper service of the equipment shall be included.

3.4 A suggested replacement parts list shall be provided itemizing the materials required for proper service and maintenance of the equipment.

SECTION 4. QUALITY ASSURANCE

4.1 The supplier shall maintain a quality control and/or inspection system that will provide assurances that material and services required meets industry recognized standards in regard to workmanship, materials, processes, and finishes. Where industry standards do not exist, General Electric Company will furnish information to the supplier to assist him in his design or manufacturing efforts.

4.2 Proof of Compliance to not only this specification but also to the suppliers own detail design must be available/or furnished to General Electric Company before shipment. This proof may be in a form convenient to the supplier and should consist of actual inspection and test data. With the concurrance of General Electric Company, design calculations and detail design drawings may be acceptable in lieu of actual tests or inspections.

4.3 The supplier must furnish detailed information regarding his proposed method of assuring that his installation is satisfactory in all respects. This information must be available at least 30 days prior to scheduled completion of installation.

4.4 Packing and Packaging of material to be delivered must be consistant with the mode of transportation utilized, but in no case will less than best commercial practice be accepted. Components, parts, or units subject to damage if exposed to abnormal atmospheric conditions shall be suitably protected by packaging if possible. All items of material in this category shall be reported to General Electric Company before shipment.

4.5 General Electric Company will make visitations to the suppliers plant during all phases of this procurement for purposes of reviewing engineering, procurement, and quality status of this subcontract.

SECTION 5. TEST DATA

5.1 The subcontractor shall supply a test plan acceptable tc General Electric for demonstrating that the set of antennas will meet the requirements of Section 3. This test plan shall be submitted more than 30 days before the start of the first of the recommended tests. The format of the test plan and of the test data reports may be that which is standard practice of the subcontractor, subject only to the requirement that the format be readily comprehensible to a reasonably competent engineer and be reproducible so that copies can be obtained of those portions considered by General Electric to be needed at General Electric.

5.2 Test data demonstrating compliance with the impedance specification may be taken during a trial erection at the subcontractors plant if the antenna is not installed by the fabricating subcontractor. The final acceptance test data on impedance will be taken after erection on the site.

5.3 Compliance with the gain and pattern requirements may be demonstrated on a model, by reference to data from previous installations, or by computations. The approval by General Electric of the use of such data or computations is required and will be based upon the judgement of the responsible General Electric engineer of the applicability and quality of the available data.

5.4 Compliance with the transmitting power requirements for the antenna may be demonstrated by reference to previous experience, subject to verification within six months after installation by test conducted by General Electric on the final installation.

5.5 The compliance of any "balun" or other transformer with the power requirement may be demonstrated by data on a previous identical unit or by direct test; however, acceptance on the basis of such data is conditional and subject to verification by tests conducted by General Electric within six months of delivery.

SECTION 6. PREPARATION FOR DELIVERY

All equipment shall be prepared for shipment in accordance with good commercial practice. Shipment shall be by commercial carrier.

SECTION 7. CHANGES

7.1 Delete paragraphs 2.3 and 3.4

7.2 Delete last sentence of first paragraph of 3.2.3

The ground contours are as shown in Figures 81, 82, and 83 (SK 62667-782-16, 17, and 18). Profiles appear in Figures 84, 85, and 86 (SK 62667-782-13, 14, and 15). Screen elevations shall be as follows:

Direction	Elevation at near tower (feet)	Slope (percent)
Panama	1779	6
Azores	1797	4 3/4
Thule	1776	4 3/4

(Note that the rear tower line is 50 feet forward from the staked baselines for Thule and Azores, and 100 feet forward for Panama.)

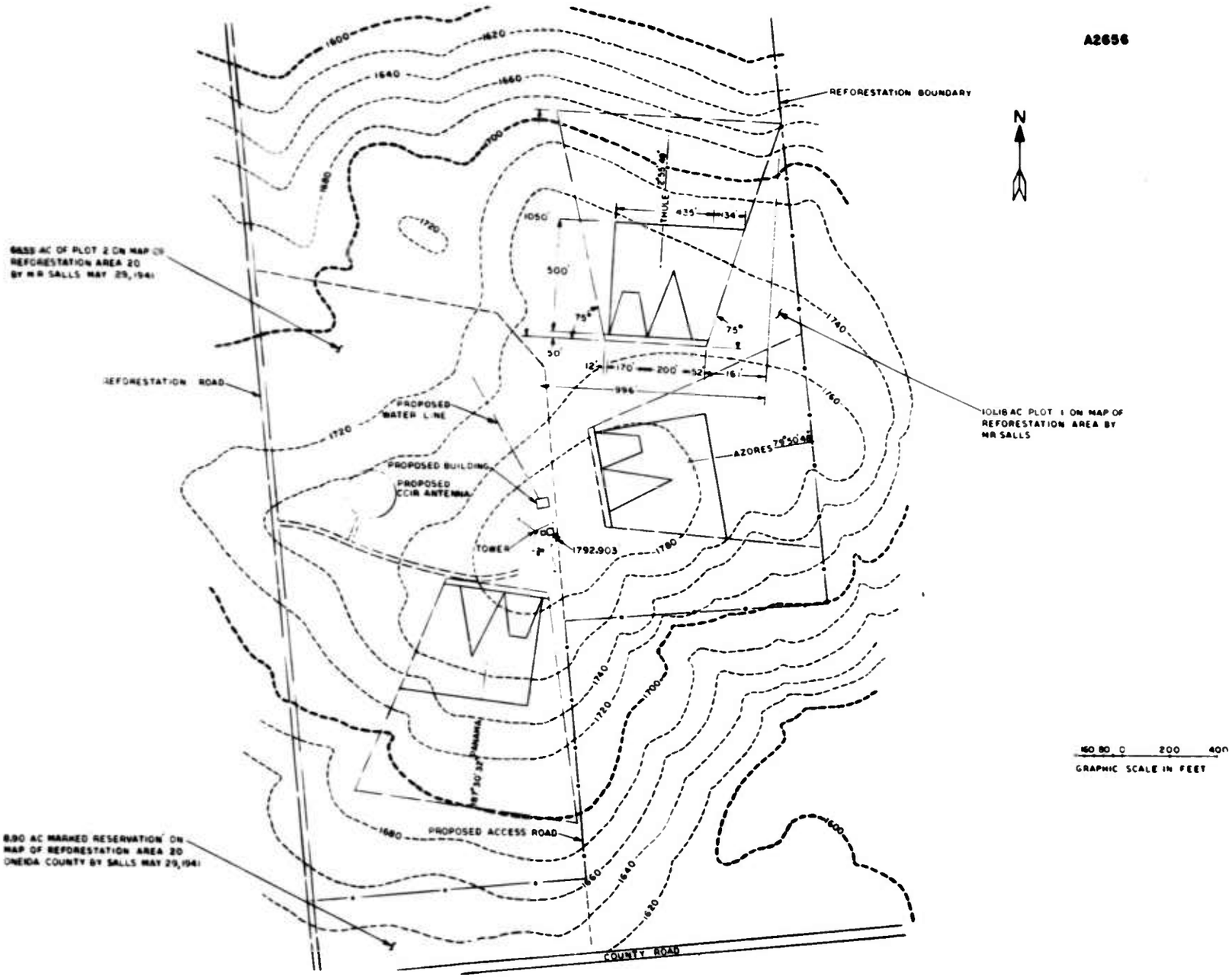


Figure 80. Starr Hill Site

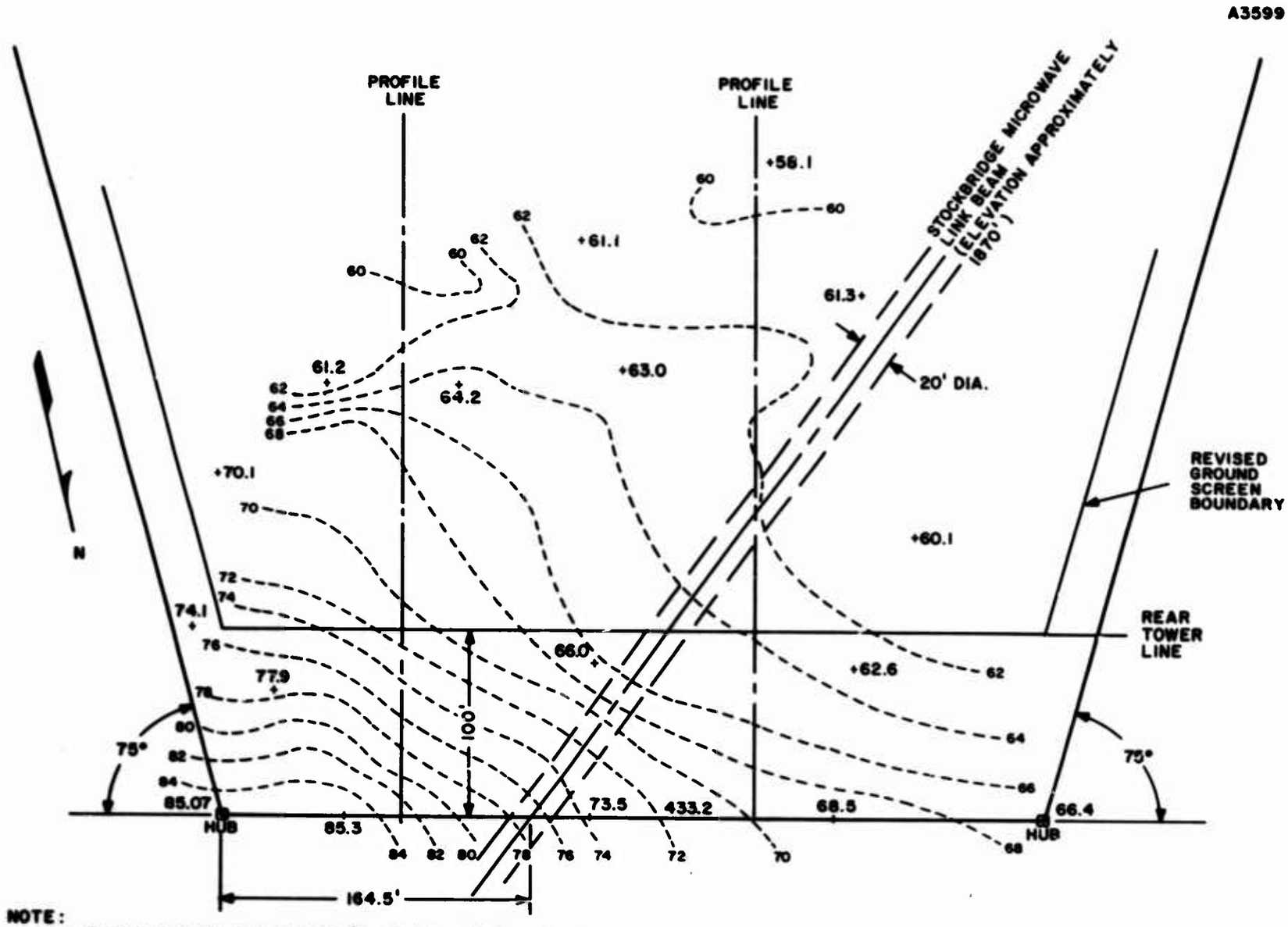
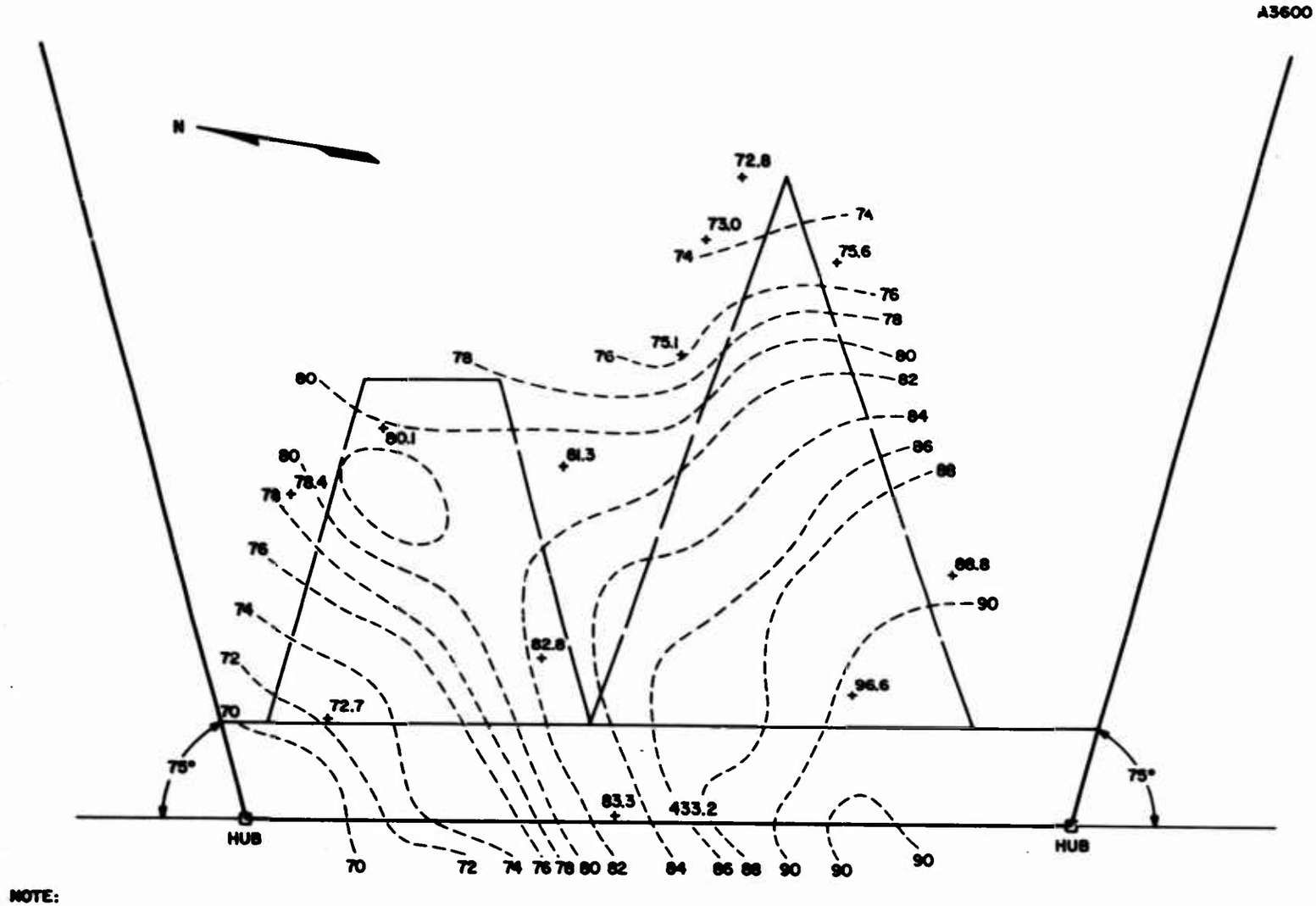


Figure 81. Topography for Panama Antenna Layout (SK 62667-782-16)



NOTE:

ALL ELEVATIONS SHOWN ARE 1700' PLUS (EXAMPLE: 1770)
x72.7 INDICATES SPOT ELEVATION.
CONTOUR INTERVAL = 2'

Figure 82. Topography for Azores Antenna Layout (SK 62667-782-17)

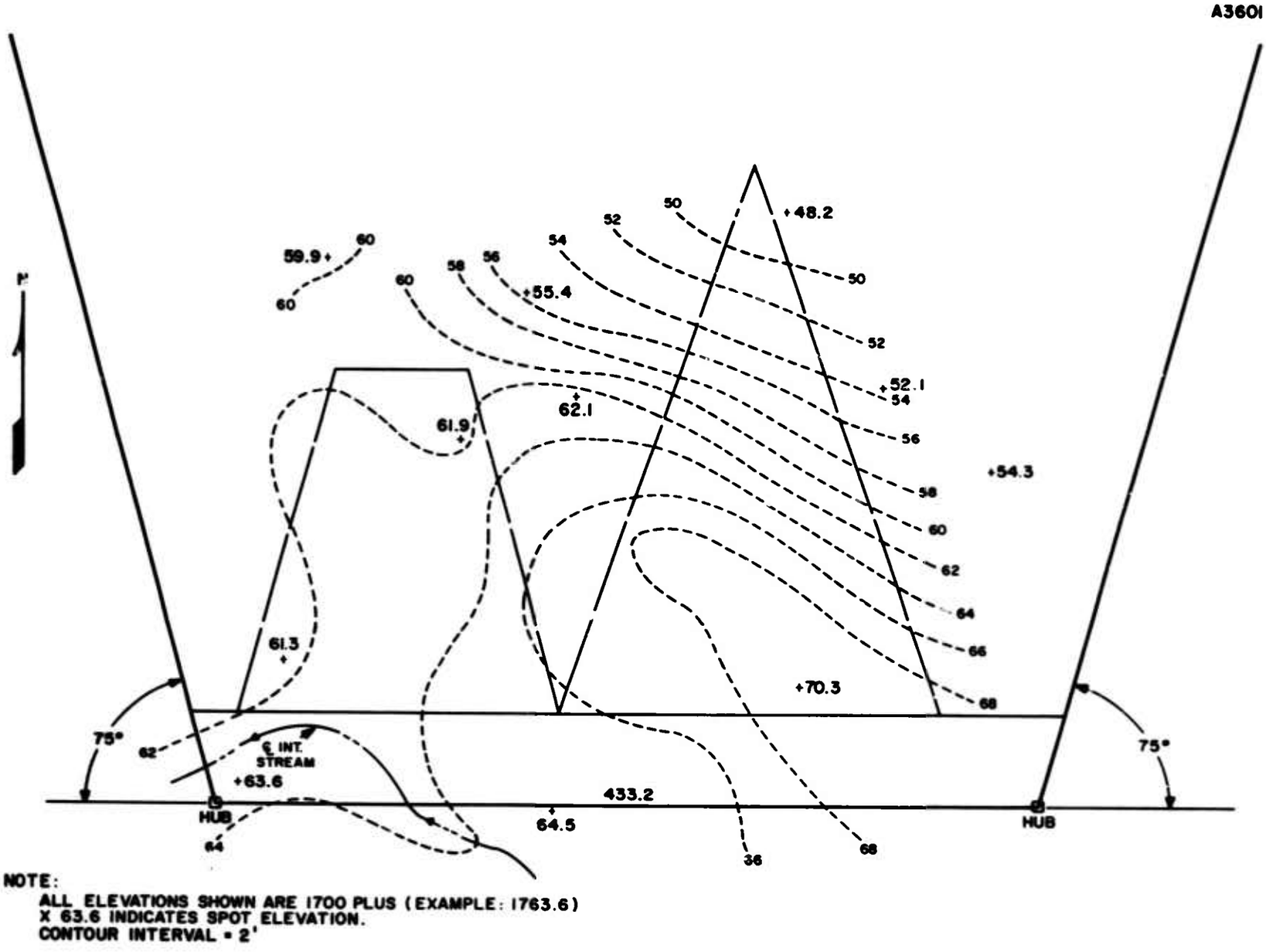


Figure 83. Topography for Thule Antenna Layout (SK 62667-782-18)

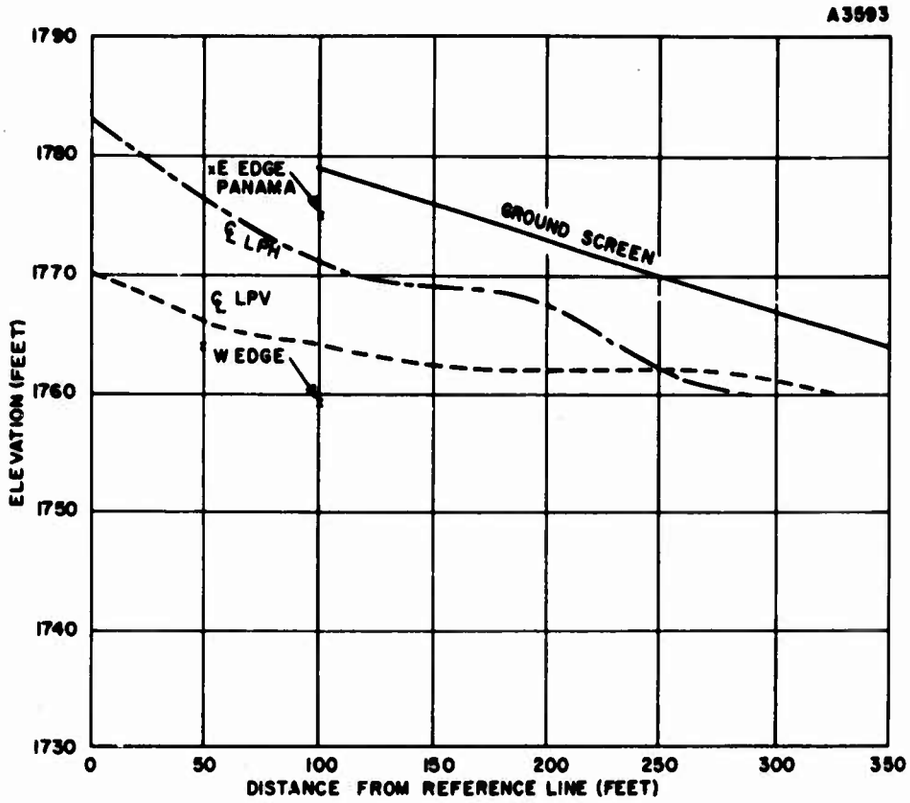


Figure 84. Panama Antenna Area Profiles (SK 62667-782-13)

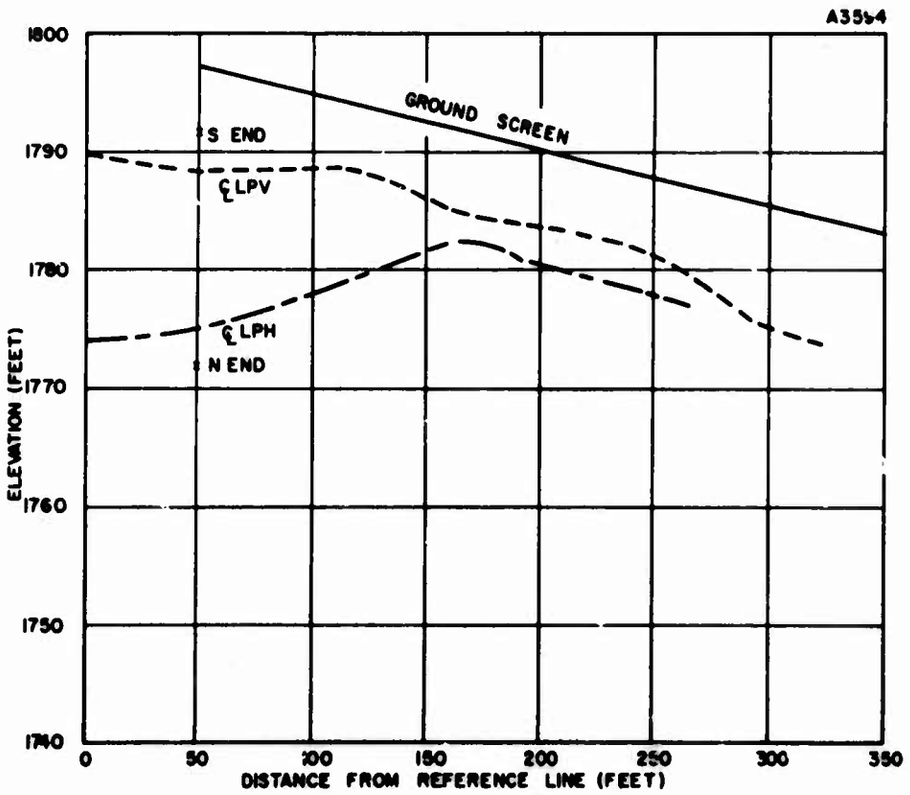


Figure 85. Azores Antenna Area Profiles (SK 62667-782-14)

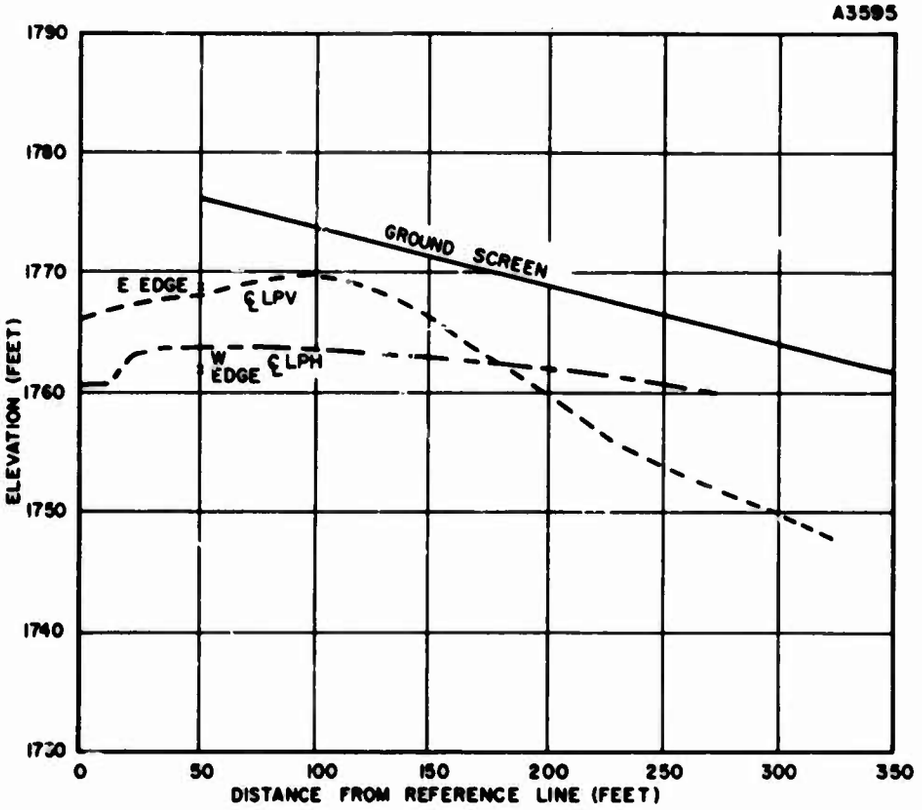


Figure 86. Thule Antenna Area Profiles (SK 62667-782-15)

APPENDIX B

SNOW ON THE GROUND SCREEN

The effect of snow and ice is not normally considered in the selection of antenna sites and in the treatment of the antenna subsystem. The antenna subsystem includes the antenna surroundings for a considerable distance when low angles of radiation are concerned. Vertical polarization is normally employed for installations where low angle radiation (down to a few degrees) is required. One of the most important requirements which must be met in order to have good low angle performance is an extensive high-conducting ground. Sea water is a good ground; therefore, a seaside location provides excellent performance, as demonstrated in actual experience. However, when sea water is covered by even a fraction of a foot of ice, performance is greatly degraded. Similarly, when a large metallic ground screen is placed in front of an antenna at an inland site, snow on the screen introduces an effect similar to that of a poor ground.

Computations have been made of the effect of a dielectric layer on top of an infinite, lossless, ground screen. This very simple model is adequate to demonstrate the necessity for including the consideration of ice and snow when planning the installation of vertically polarized antennas for low angle performance. The results of some computations are given in Figures 87 through 91. These are computations for both packed wet snow and light fluffy snow of considerably greater depth (conditions representative of those found at Starr Hill). The results for ice are in general similar to those of packed snow.

The first two figures show the effect of packed snow. The presentation is the loss introduced by the snow as a function of frequency and elevation angle. As will be noted, at 4 MHz, there is relatively little effect; however, for an angle 2° above the ground screen, the introduction of one foot of packed snow (a very common condition at Starr Hill) can introduce more than 11 dB of attenuation at 32 MHz. Two feet of snow is also entirely possible at this location. The loss for the 2° elevation angle goes beyond the range of the graph at 32 MHz. At lower frequencies -- 8 MHz and below -- for shallow depths of snow, corrections could probably be made to the computed or measured patterns to allow for the effect of snow. At the higher frequencies, however, it is improbable that the snow conditions would be well enough known to permit corrections of any reasonable accuracy.

Loose snow can readily accumulate to a depth of four to six feet at Starr Hill. Figures 89, 90, and 91 present the data on loss as a function of snow depth for the frequencies of interest. Again it is noted that at 4 MHz, the effect is relatively small even down to the 2°

elevation angle. At 8 MHz the effect becomes considerable and the ability to introduce corrections would become poor. The loss is progressively more at 16 and 32 MHz, and of course, at 64 MHz, the loss introduced is very great even at higher elevation angles such as 10°. It should be noted that the point at which the field strength was computed for determining these curves was below the surface of the snow at the six-foot depth at 64 MHz, so these points are of questionable validity. The conclusion reached as a result of this study was that it would be necessary to raise the ground screen above the ground to a height such that snow could not accumulate above the ground screen. Practical considerations such as access under the ground screen area have dictated a height of approximately eight feet above the ground.

The computations on which Figures 87 through 91 are based were actually the computations of field intensity at a height one-quarter wavelength above an infinite ground screen. The snow was represented as a lossless dielectric with a relative dielectric constant of 2.25 for packed snow, and 1.2 for loose snow. The field strength was taken at the one-quarter wavelength height as a reasonable representation of what would happen to a log-periodic dipole antenna located with the lower ends of the dipoles essentially at the ground screen.

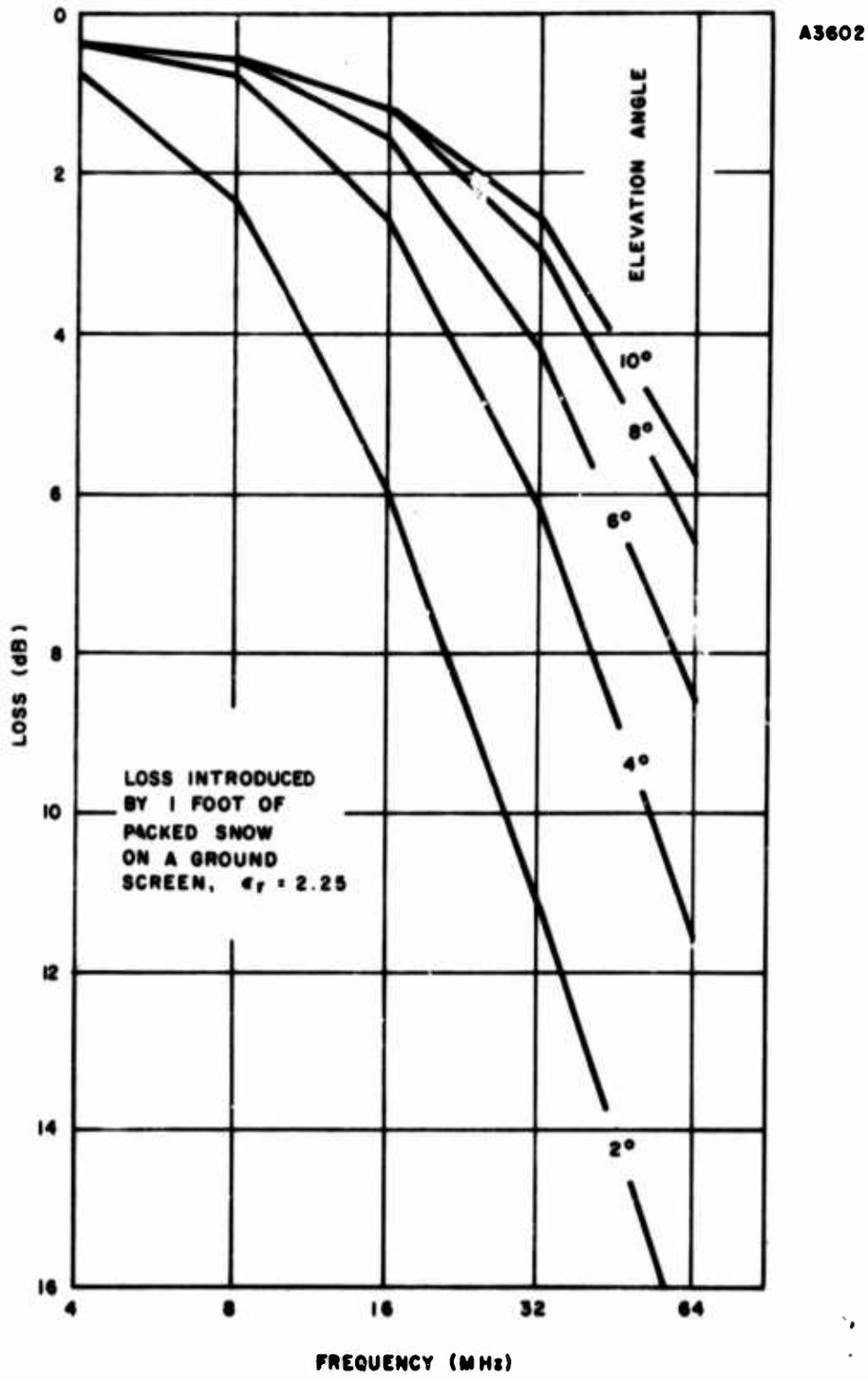


Figure 87. Loss Introduced by One Foot of Snow on a Ground Screen

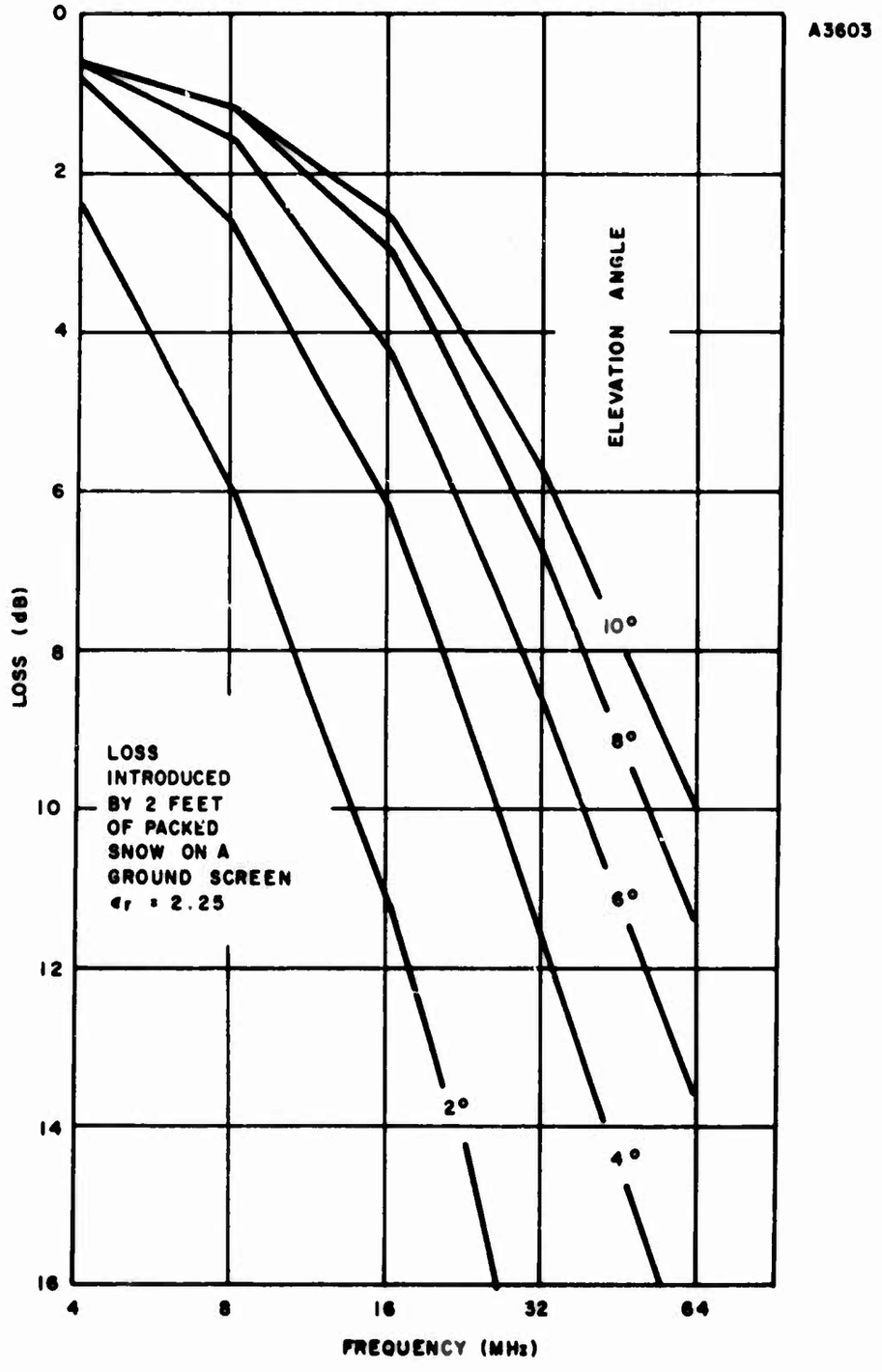


Figure 88. Loss Introduced by Two Feet of Snow on a Ground Screen

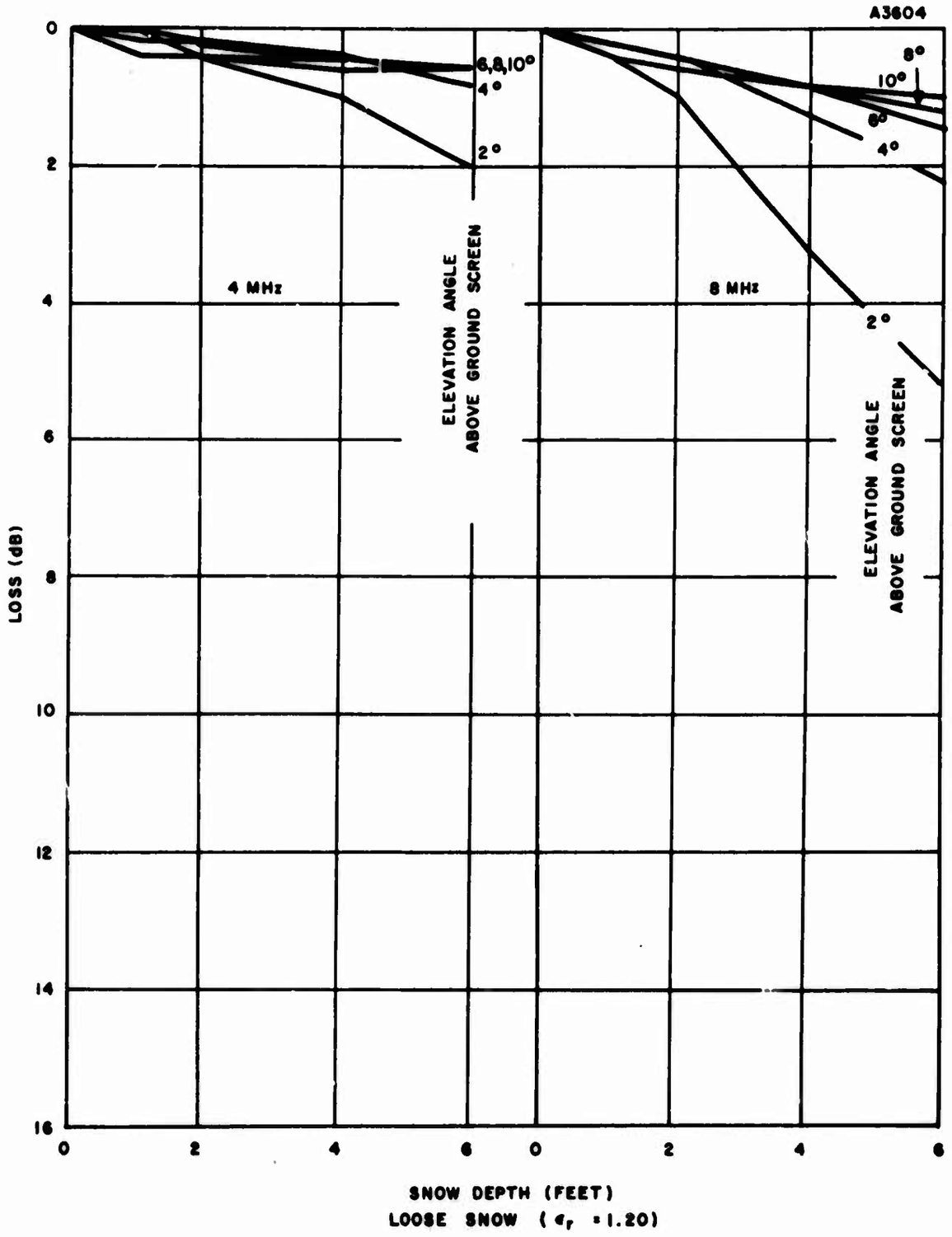


Figure 89. Loss Introduced by Loose Snow on a Ground Screen, 4 and 8 MHz

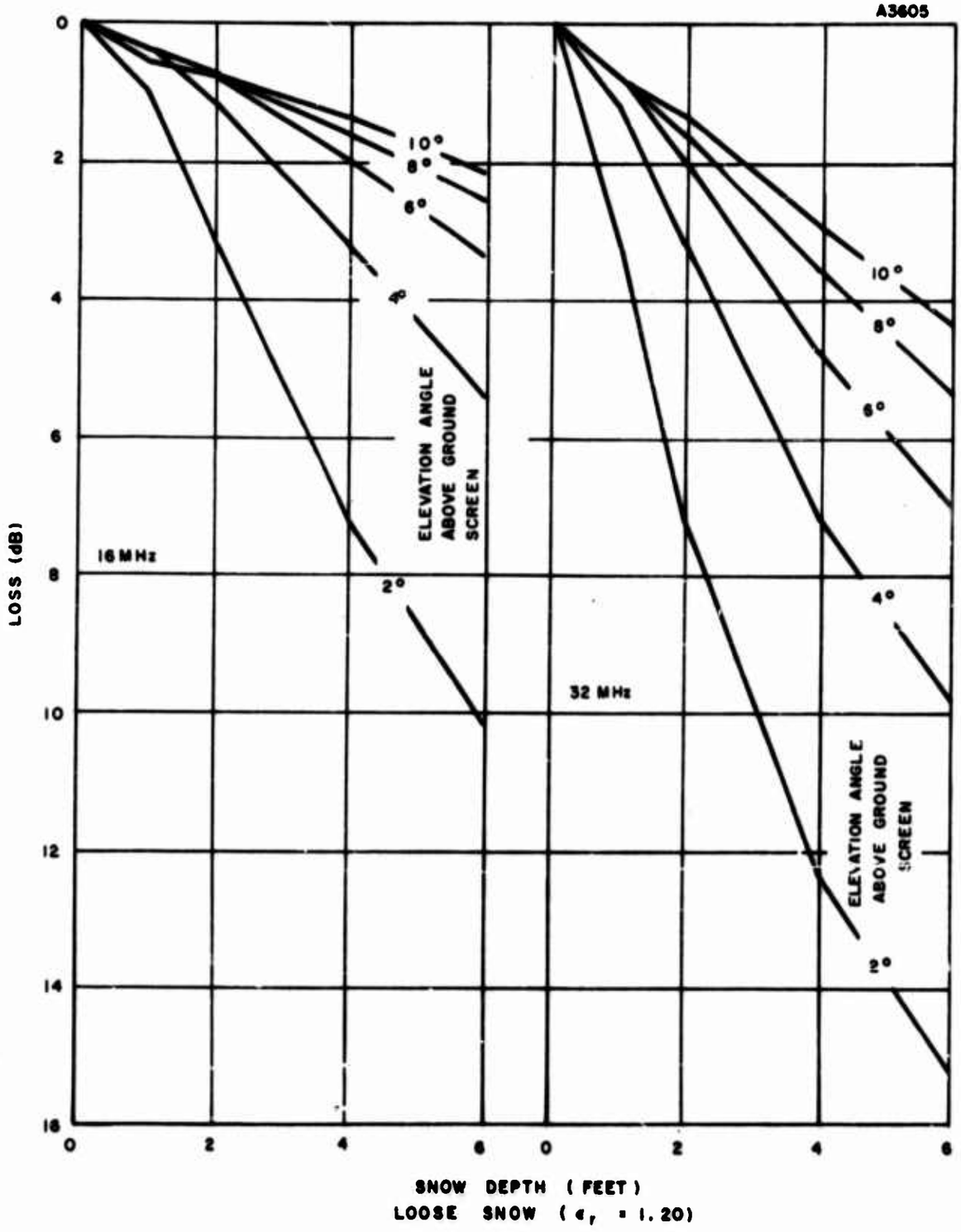


Figure 90. Loss Introduced by Loose Snow on a Ground Screen, 16 and 32 MHz

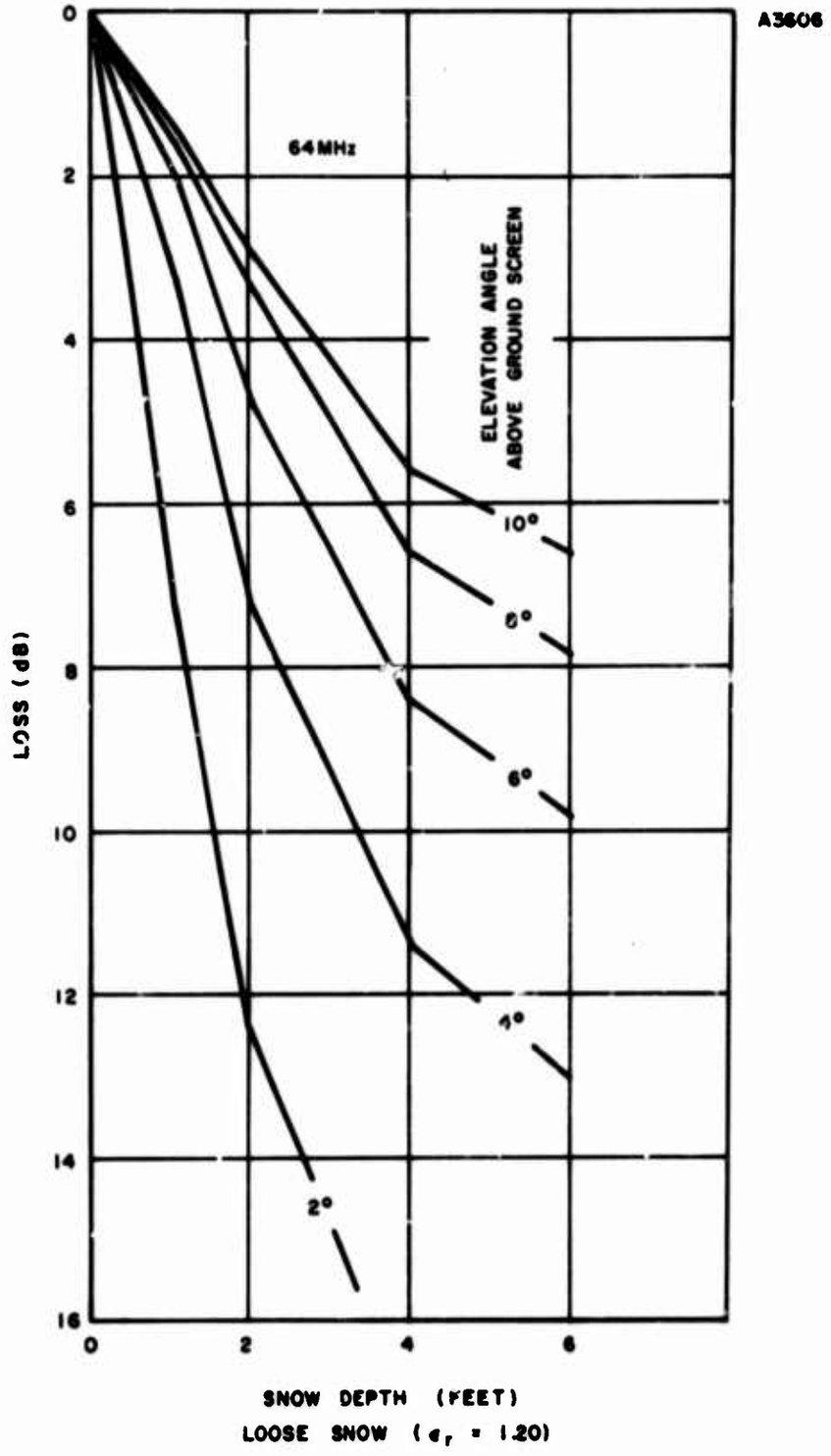


Figure 91. Loss Introduced by Loose Snow on a Ground Screen, 64 MHz

APPENDIX C

WORK SPECIFICATION
FABRICATION OF COPPERWELD GROUND SCREEN

1. SCOPE OF WORK

The seller will fabricate approximately 864,000 square feet of copperweld ground screen with a mesh size of two by two feet. The screen will be made in 96 mats, each 500 feet long and 18 feet, 4 inches wide (as described in Figure 92), using No. 10 AWG copperweld wire. The copperweld wire will be furnished to the seller. The ground screen mats will be fabricated with a tolerance of ± 1/4 inch in five feet of length. The seller will endeavor to hold the accumulated error to a minimum. The manufacturing tolerances in mesh size will be ± 1/4 inch, in mat width ± 1/2 inch, and in overhang ± 1/4 inch.

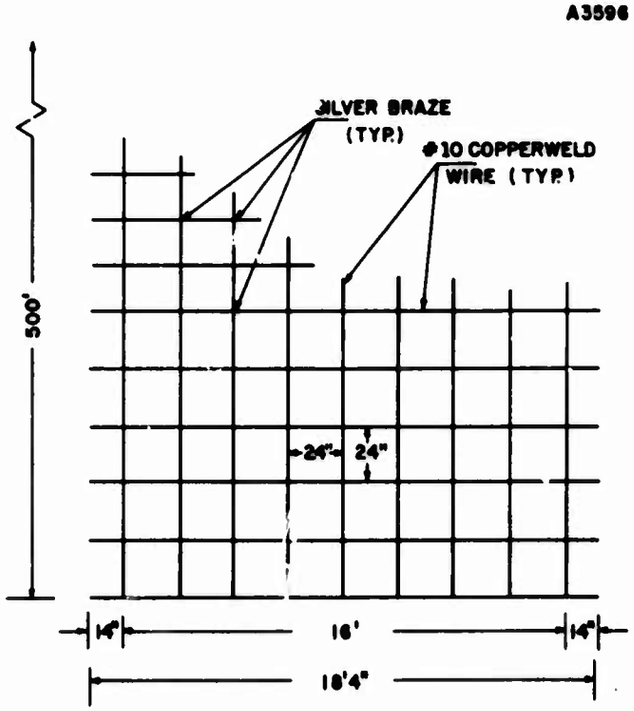


Figure 92. Typical Plan, 18-Foot Ground Screen Mat

All cross wire and lap silver brazed connections must meet the test specifications stated in paragraph below, and ASTM Specification B-260 (BCuP5 or BAg-2). The flux used in the silver brazing processing will be an in-line gaseous flux. This flux shall be used in such a manner that no corrosive residual flux will remain on the wire and joints. As a result, no corrosion will be caused by the flux used in the performance of this work. The copper coating which is destroyed or found to be defective during manufacture, shall be recoated with silver brazed material.

The manufactured ground screen shall be rolled in a one-foot minimum diameter and will be commercially packed in such a way as to prevent damage during shipment by surface transportation.

2. INSPECTION AND ACCEPTANCE

The seller will perform and record the following Quality Assurance Tests. Records of these tests and four tagged test samples (three cross wire and one lap joint) from each roll will be made available to the Government and/or General Electric inspectors upon request.

All silver brazed connection samples shall be tested as follows:

1. CROSS WIRE TENSILE TEST shall be made by pulling the through wire with a cross wire silver brazed to it. The tensile strength of the through wire shall be equal to or greater than the minimum strength of the parent wire in the annealed condition.

Wire Size	Wire Type	Min. Strength
No. 10 AWG	30% Copperweld	472 lbs.

2. LAP JOINT TENSILE TEST will be made in the same manner and with the same minimum strength as in 1. above.

3. A PEEL STRENGTH TEST shall be made by bending each wire at the silver brazed connection around a one-inch mandrel until the wires are parallel. When both ends of each wire are gripped and the load on a silver brazed connection is applied, the breaking strength shall be a minimum of 60 percent of the wire strength shown in 1. above. This test is not valid if the wire breaks before the brazed connection breaks and, therefore, will be marked 'invalid' in each case where this happens. Ten percent of the test samples may have a breaking strength of ten percent lower than that specified above.

4. A RESISTANCE TEST shall be made by comparing the resistance of a gage length of the parent wire to the resistance across the same gage length and through the silver brazed connection. The resistance across the silver brazed connections shall be no greater than that of the parent wire.

The Seller will perform such in-process and final inspections as are required to assure that all connections are properly made, all excess flux removed, and no steel core remains exposed.

The fabricated ground screen will be accepted after final inspection at the Seller's plant by General Electric and/or Government Inspectors. Shipping instructions will be provided by the General Electric Company buyer.

Final G.E. and/or Government inspection will primarily consist of checking the seller's inspection records, connection samples, packaging, and labeling. Inspection for quality of workmanship and tolerances normally will be made while individual mat rolls are being fabricated (in-process inspection).

3. GOVERNMENT FURNISHED PROPERTY

The seller will be provided with 960,000 linear feet of No. 10 AWG copperweld wire in 6000-foot rolls. All excess and scrap wire will be returned with the last ground screen shipment.

The seller will maintain records of the GFP wire received, the amount of wire used in the manufacture of the ground screen, and the scrap and the surplus returned with the last ground screen shipment.

The GFP wire provided to the seller is in a tarnished condition. The seller will have the GFP wire cleaned as authorized so that the wire is in a new condition (clean, untarnished, and uncoated).

APPENDIX D

WORK SPECIFICATION
INSTALLATION OF STARR HILL GROUND SCREENS

1. SCOPE OF WORK

The work involves the assembly and erection of three separate ground screens made from 32 rolls each of 2-foot by 2-foot mesh on land previously logged within 8 inches above ground. Each ground screen will be supported by vertical poles located in a square grid fashion 18 by 18 feet and over horizontal studs nailed to the poles. The parallel rows of studs will be across the width of the screen as shown in Figures 93 and 94.

2. GENERAL PROVISIONS

Material supplied by the General Electric Co. will consist of 96 rolls of mesh 18 feet, 4 inches wide by 500 feet long. The mesh size is 2 feet by 2 feet made from 0.104-inch diameter copper over steel wire (commonly known as telephone wire) with welded cross joints. The General Electric Co. will also provide 30,000 compression fittings and 6 hand tools. The hand tools will be returned to the General Electric Co. upon completion of the work.

The contractor will supply all poles, studs, fasteners, nails, tools, and any other equipment necessary for the accomplishment of the work outlined herein.

1. All poles will be ASA Southern Yellow Pine, not framed, class 7, fully treated with 8#/cu. ft. grade one creosote.

2. All studs will be construction grade 2-inch by 2-inch by 20-foot White Fir per 323-b of Western Wood Products Association Grading Rules. Studs will be kiln dried.

Transportation of all supplies and equipment wherever such are needed will be provided by the contractor.

The contractor will take all necessary precautions to prevent damage or misalignment to existing antenna structures.

3. DESCRIPTION OF WORK

The contractor will effect a continuous, mechanically secure ground screen for all three areas which will meet the following requirements:

1. Ground screen designated as Panama will start at an elevation of 1779 feet and have a downward slope of 6 percent.

2. Ground screen designated as Thule will start at an elevation of 1776 feet and have a downward slope of 4-3/4 percent.

3. Ground screen designated as Azores will start at an elevation of 1797 feet and have a downward slope of 4-3/4 percent.

4. The start of all ground screens will be in line with existing antenna towers and referenced in elevation to existing bench marks.

5. Vertical poles will have minimum groundline distances from butt as follows:

Length of Pole (feet)	Distance (feet)
12	2.5
14	3
16	3.5
18	3.5
20	4
22	4.5

Note: Wherever boulders are encountered which are deemed by the contractor as being too large to affect practical removal, an equivalent pole support will be devised above the boulder.

6. Adjacent rolls of mesh will be joined by applying one of the compression fittings provided, at each two-foot spacing using the compression tool.

7. The horizontal studs will be nailed to the poles through the four-inch side and to each other through the two-inch side in an alternating fashion as shown in Figure 94.

8. The ground screen shall be fastened to the horizontal studs at four 4-foot spaces and in such fashion as to keep the screen from lifting but not to prevent lateral motion in any direction. A suggested method for doing this is shown in Figure 94.

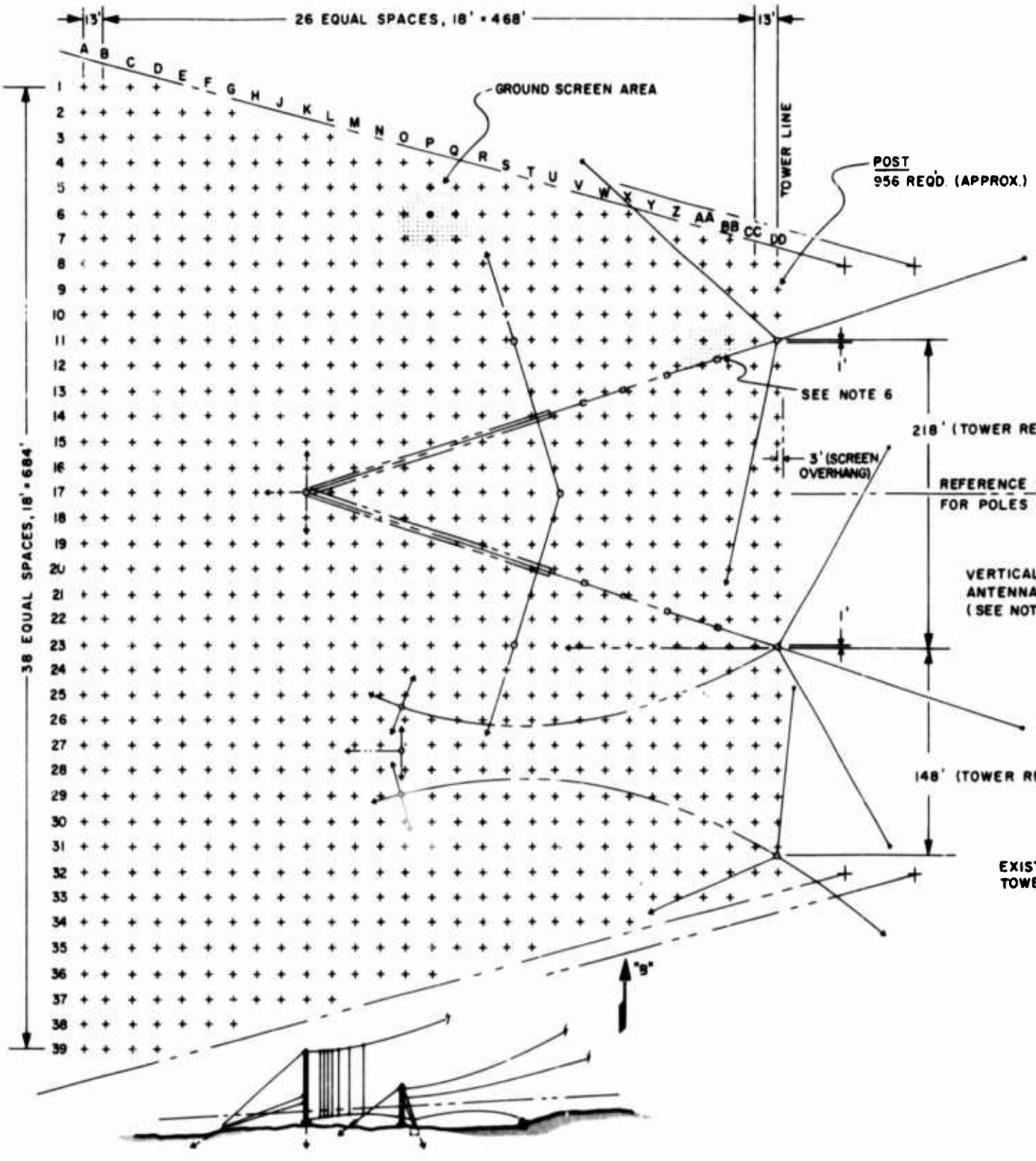
Note: The use of metallic fasteners is not recommended where such use results in sliding metal to metal contact. The screen will further be fastened along the stepped sides in like manner by using either a messenger wire or nailing cross two- by four-inch members to the poles.

4. TOLERANCES

The slope plane for each ground screen will lie within a tolerance zone of plus or minus one inch from true position; that is, the plane intersecting the poles for the location of the studs will lie between two imaginary planes two inches apart.

In order to keep the pole lengths to a minimum, it will be permissible -- subject to General Electric Co. approval -- to increase the slope of the ground screen, hinging at a

line parallel (within four feet) to the antenna tower line. Such hinging is to occur beyond the front of the vertically polarized antenna and shall be limited to the degree that the ground screen will not be any closer than four feet to any portion of the remaining ground screen area. Approval from a cognizant General Electric engineer must first be obtained by the contractor prior to deviation in the continuous ground screen slopes as specified in 3-3.


13'
26 EQUAL SPACES, 18' • 468'
13'
A B C D E F G H J K L M N O P Q R S T U V W X Y Z AA BB CC DD
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
38 EQUAL SPACES, 18' • 684'
GROUND SCREEN AREA
TOWER LINE
POST
956 REQD. (APPROX.)
1'
SEE NOTE 6
218' (TOWER REF.)
3' (SCREEN OVERHANG)
REFERENCE LINE FOR POLES
VERTICALLY PO
ANTENNA.
(SEE NOTE 6)
1'
148' (TOWER REF.)
EXISTING AN
TOWERS AN
"9"

Fig

1

A3597

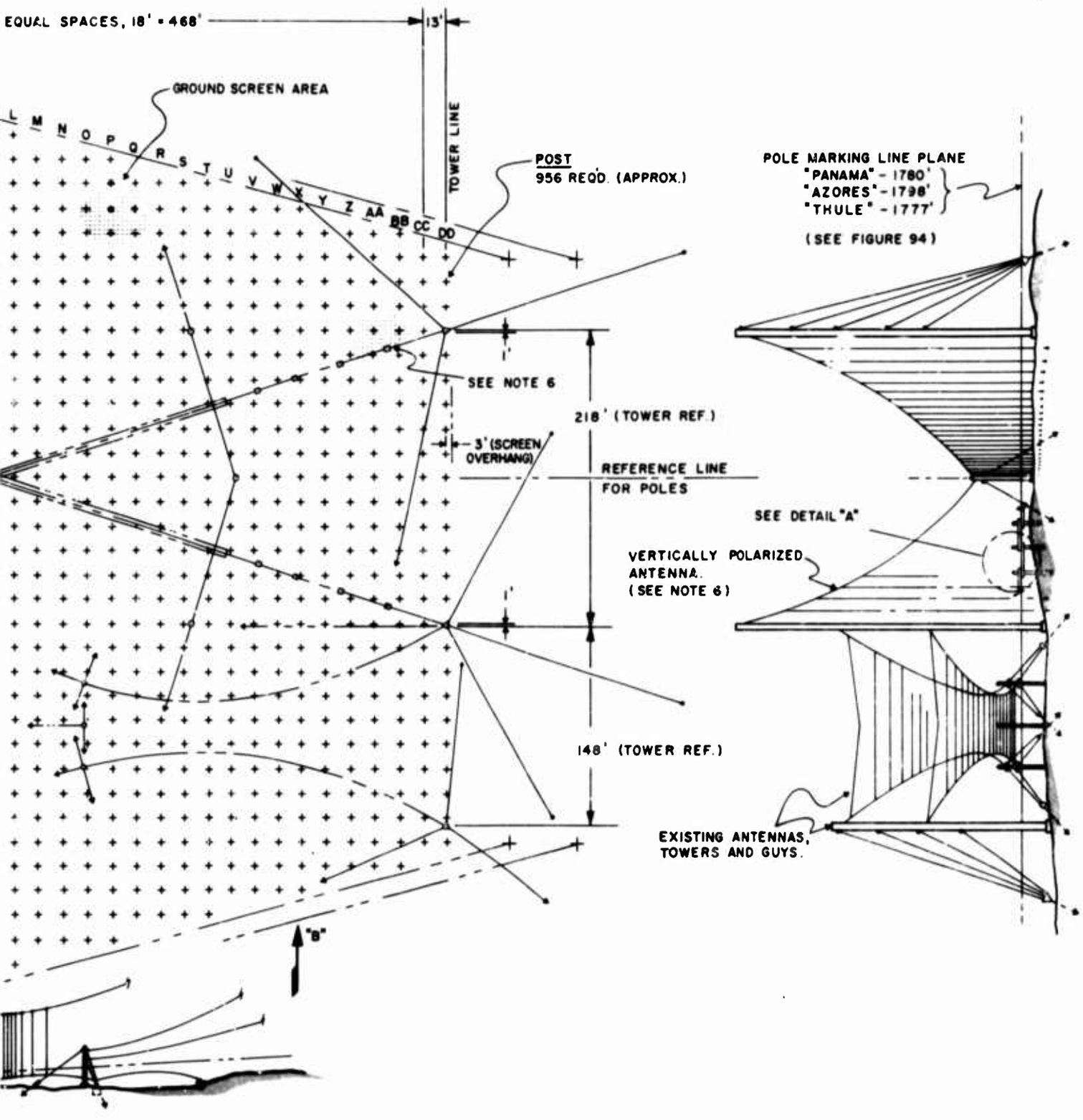
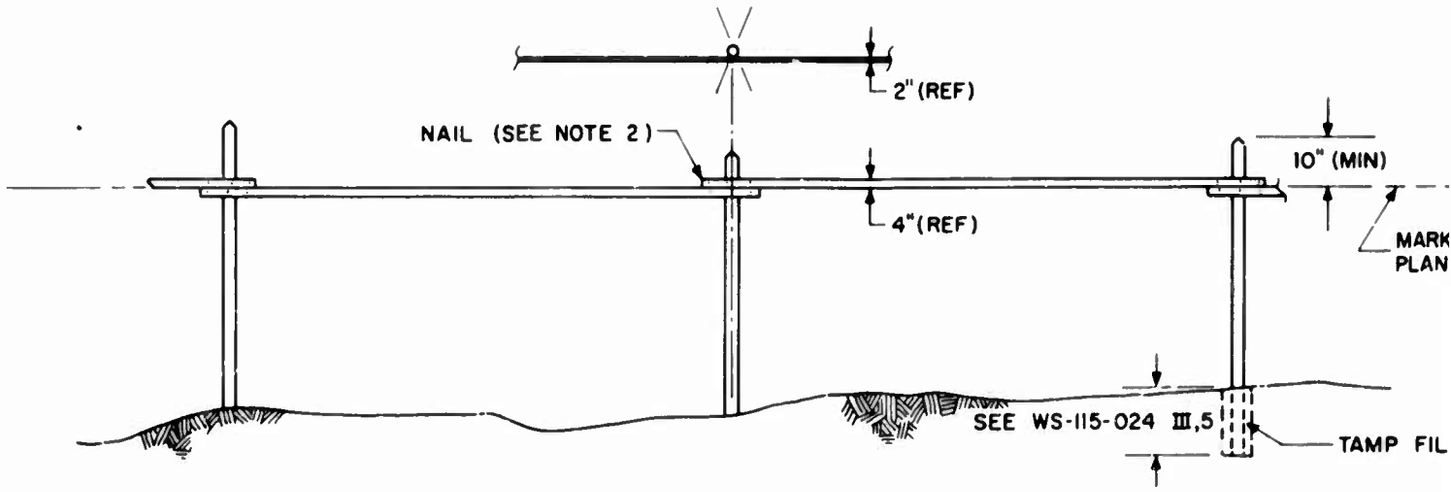
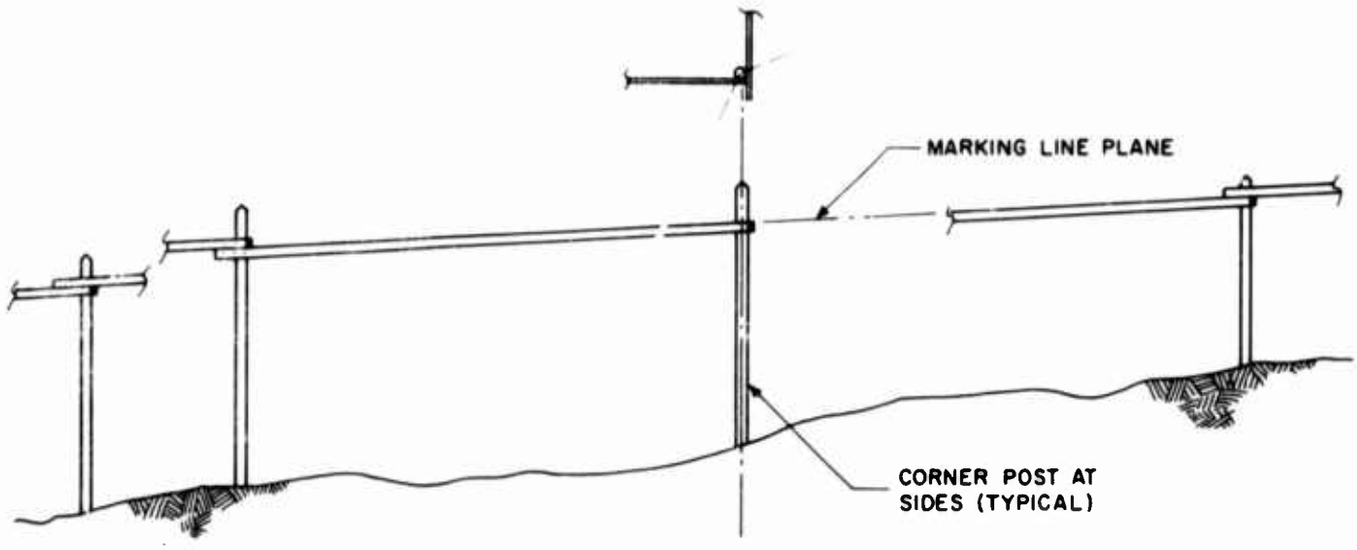


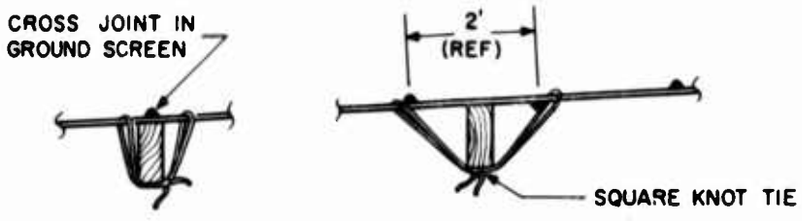
Figure 93. Ground Screen Layout

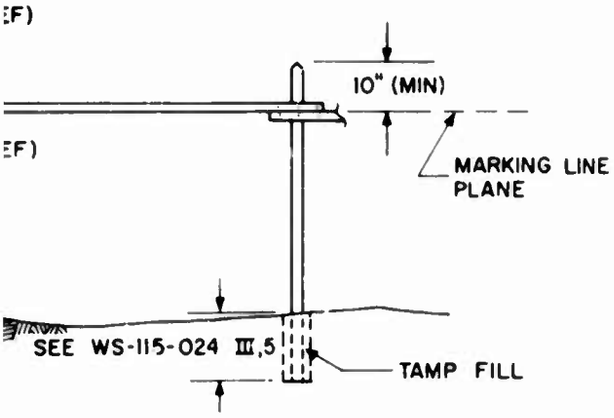


DETAIL "A" (ELEVATION)



DETAIL "B" (ELEVATION)





NOTES:

1. ALL POSTS TO BE PLUMB WITHIN 1/4" PER FOOT OF LENGTH ABOVE GRADE.
2. NAILS TO BE NO LESS THAN 20-PENNY SIZE, ROSIN-COATED WITH A MINIMUM QUANTITY OF 4 PER DOUBLE STUD JOINT.
3. WHERE IT APPEARS THAT NAILING WILL AGGRAVATE EXISTING SHAKES AND/OR SPLITS AT THE ENDS OF A STUD; OR WHERE IT APPEARS THAT SUCH SPLITTING WILL OCCUR BECAUSE OF RADIAL GRAIN POSITION THEN IT WILL BE REQUIRED THAT THE STUD BE PREDRILLED.
4. TIE DOWN MATERIAL SHALL BE BRAIDED DACRON (OR EQUIV.) 100-LB TEST.
5. OMIT POSTS AT THE FOLLOWING LOCATIONS: DD-11, DD-23, N-16, N-18, Q-15, Q-19, Q-27, O-29, V-17.
6. MAINTAIN 2' CLEARANCE (MIN.) AROUND ELEMENTS OF VERTICALLY POLARIZED ANTENNAS.

Figure 94. Ground Screen Details

REFERENCES

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7. Frequency and Time Standards, Hewlett Packard Company, Application Note 52, November 1965.

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10. Dispersive Characteristics of the Ionosphere, Interim Report No. 5, Contract AF30(602)-3360, General Electric Company, Syracuse, N.Y.

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13. ABSTRACT

This interim report includes discussions on the work performed by the General Electric Company in providing new instrumentation for the Expanded Little IDA Program. The prime objective of this program is the collection and analysis of H.F. propagation data that will aid in the design and operation of over-the-horizon radar systems. The equipment discussed in this report will be utilized to meet this objective. This third interim report describes work performed from 15 March 1966 to 15 September 1966.

The new instrumentation discussed herein includes equipment required at (1) the Starr Hill, New York central receiving site; (2) the Coco Solo, Canal Zone transmitting site; and (3) the two new transmitting sites. Specific equipment discussed in this report includes HF antennas, a high dynamic range HF receiver, digital and mode processors, absolute timing system, ionospheric sounders, Phantom pulse compression system, and test and communication equipment.

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14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
High Frequency Receiver Antennas Ionosphere Noise						

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